

# NB2329\_D350 V4.0 DDR4

## Intel Gemini Lake Refresh Platform

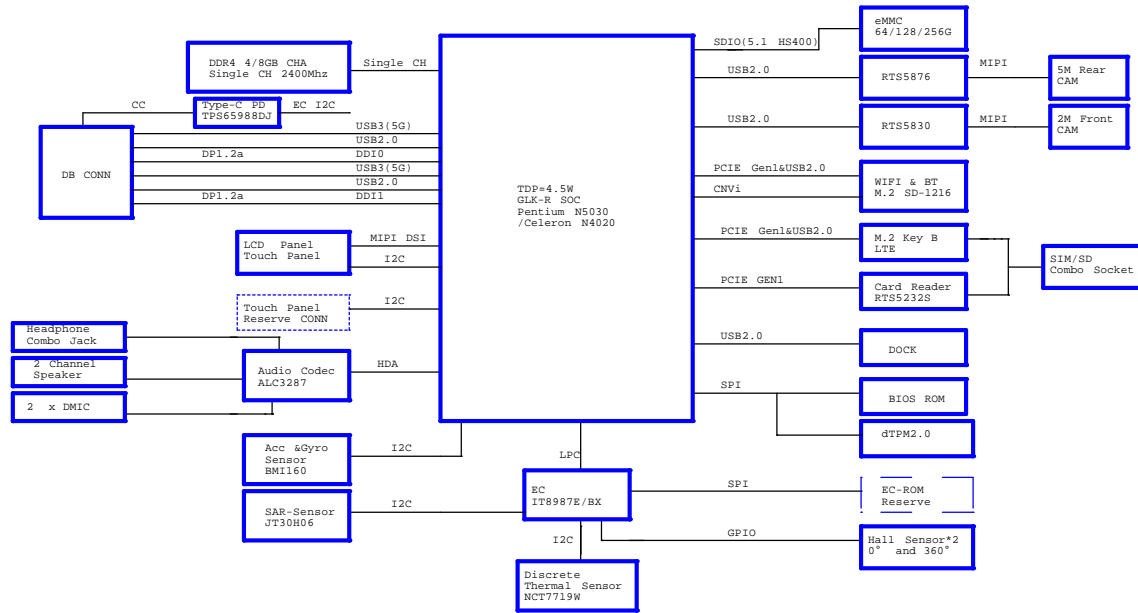
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7	SOC(eMMC/SPI/LPC/AUD/PMU)	22	FRONT CAMERA	37	TYPE C 1&2 PD TPS65988	52	CHANGE LIST
8	SOC(DDI/DSI)	23	REAR CAMERA	38	TYPE C 1&2 Power IN&OUT	53	POWER SQUENCE 1
9	SOC(I2C/CNV/LPSSSPI/UART)	24	EMMC	39	BLANK	54	POWER SQUENCE 2
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13	SOC(GND)	28	MIPI LCD CONN	43	POWER CHARGER		
14	SOC(DECAP)	29	WLAN 1216 HP2 AC	44	POWER 3.3V		
15	SOC(STRAP)	30	DOCKING POGO PIN	45	POWER 5V		



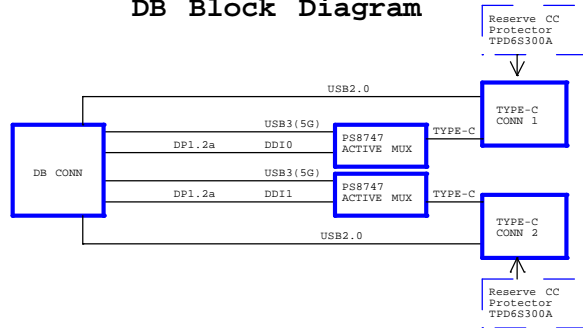
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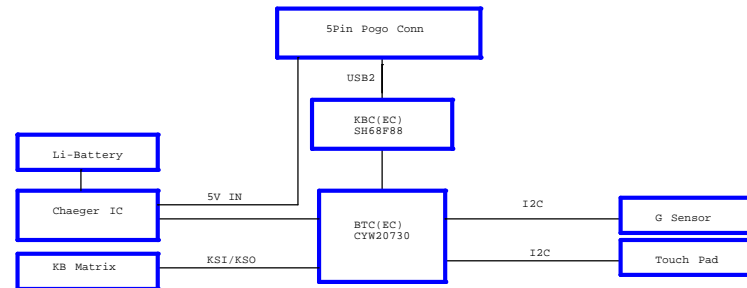
## Pad Block Diagram



## DB Block Diagram



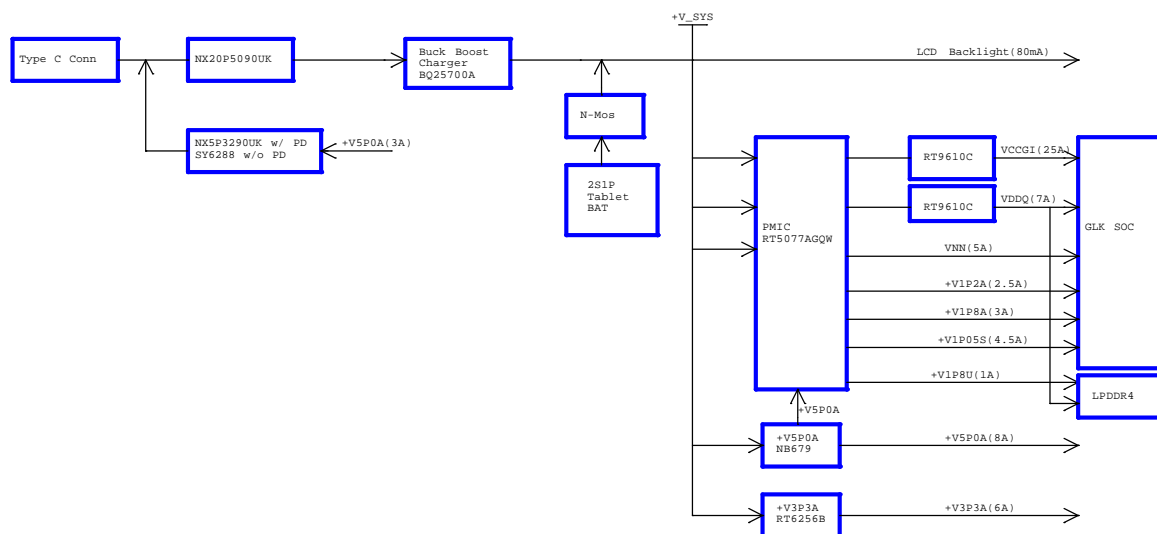
## Dock Block Diagram




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### Power States(Adapter)

Signal	SLP_S0#	SLP_S3#	SLP_S4#	+V5P0A	+V3P3A	VNN	V1P8A	V1P2A	VCGL	+V1P05S	+VDDQ
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	LOW	LOW	HIGH	ON	ON	OFF	ON	ON	OFF	OFF	ON
S4(STD)	LOW	LOW	LOW	ON	ON	OFF	ON	ON	OFF	OFF	OFF
S5(SoftOff)	LOW	LOW	LOW	ON	ON	OFF	ON	ON	OFF	OFF	OFF

### Power States(Battery)

Signal	SLP_S0#	SLP_S3#	SLP_S4#	+V5P0A	+V3P3A	VNN	V1P8A	V1P2A	VCGL	+V1P05S	+VDDQ
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	LOW	LOW	HIGH	ON	ON	OFF	ON	ON	OFF	OFF	ON
S4(STD)	LOW	LOW	LOW	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5(SoftOff)	LOW	LOW	LOW	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

### MEM ID

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	
0	0	0	0	4x Samsung 8Gb K4A8G165WC-BCWE
0	0	0	1	4x Micron 8Gb MT40A512M16TB-062E:J
0	1	0	1	4x Hynix 8Gb H5AN8G6NCJR-XNC
0	1	0	0	4x Hynix 16Gb DDP H5ANAG6NCMR-XNC
0	0	1	0	4x Samsung 16Gb K4AAG165WA-BCWE
0	0	1	1	4x Micron 16Gb MT40A1G16KNR-075:E (DDP)
0	1	1	1	
0	1	1	0	
1	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	

### LCD ID

LCD_ID1	
0	
1	

### G & A Sensor ID

	I2C_ADD_SEL
BMI160 Bogch	0
ICM-40607 InvenSense	1

### TPM/TCM ID

	GPIO105
FTPM	0
dTPM	1

### TPM ID


	GPIO140	GPIO213
新塘	0	0
Infineon/ 国民技术	1	0
ST	0	1

### HSIO Port

NO.	Device
1	USB3.0 port0 (Type-C1)
2	USB3.0 port3 (Type-C2)
3	Pcie port0 (Card Reader)
4	Pcie port1 (LTE)
5	Pcie port2 (SSD,Reserve)
6	Pcie port3 (SSD,Reserve)
7	Pcie port5 (WLAN)

### USB2.0 Port

Port	Device
0	Type-C1
1	LTE
2	BT
3	Front Cam
4	Dock
5	Type-C2
6	Rear Cam

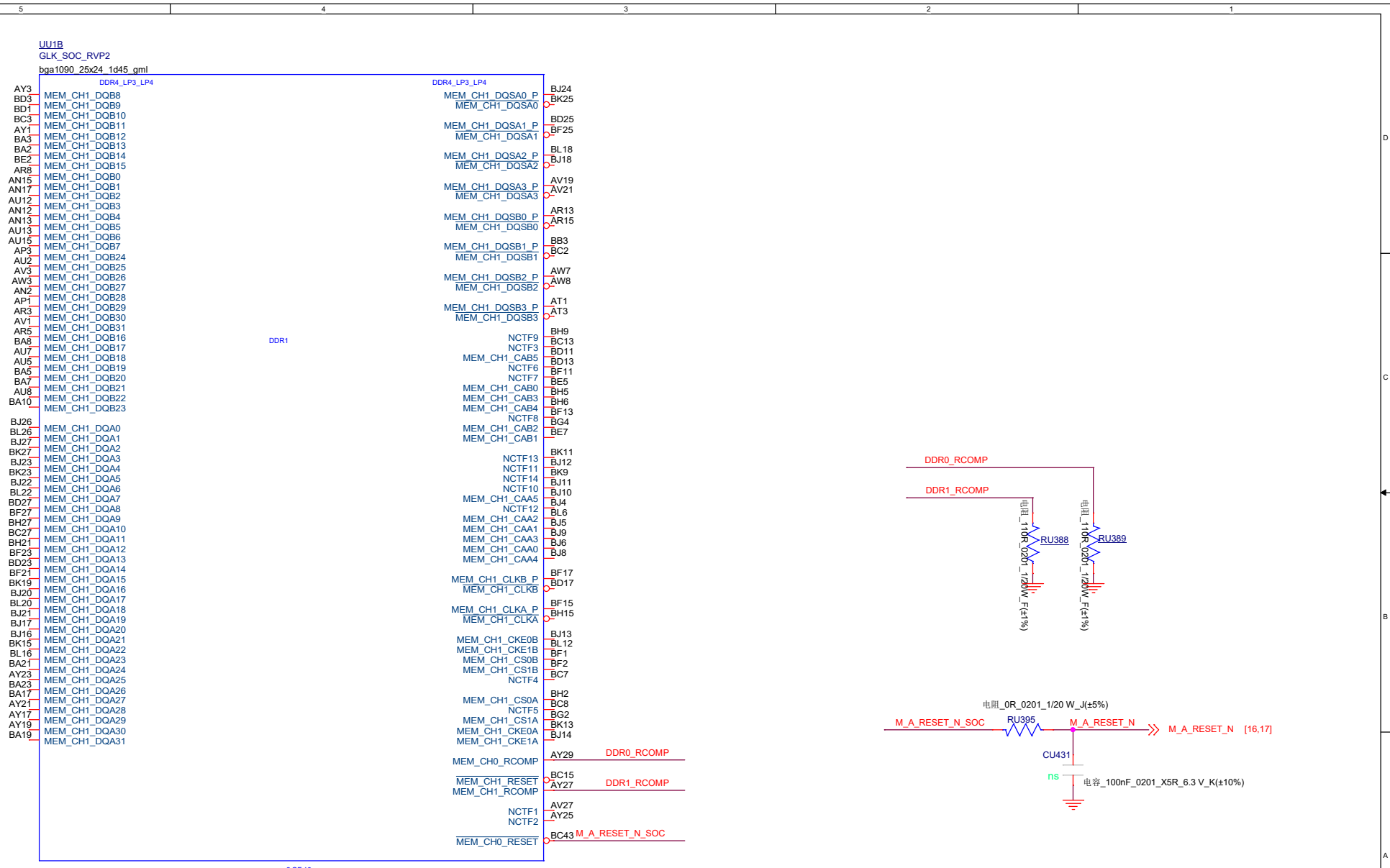
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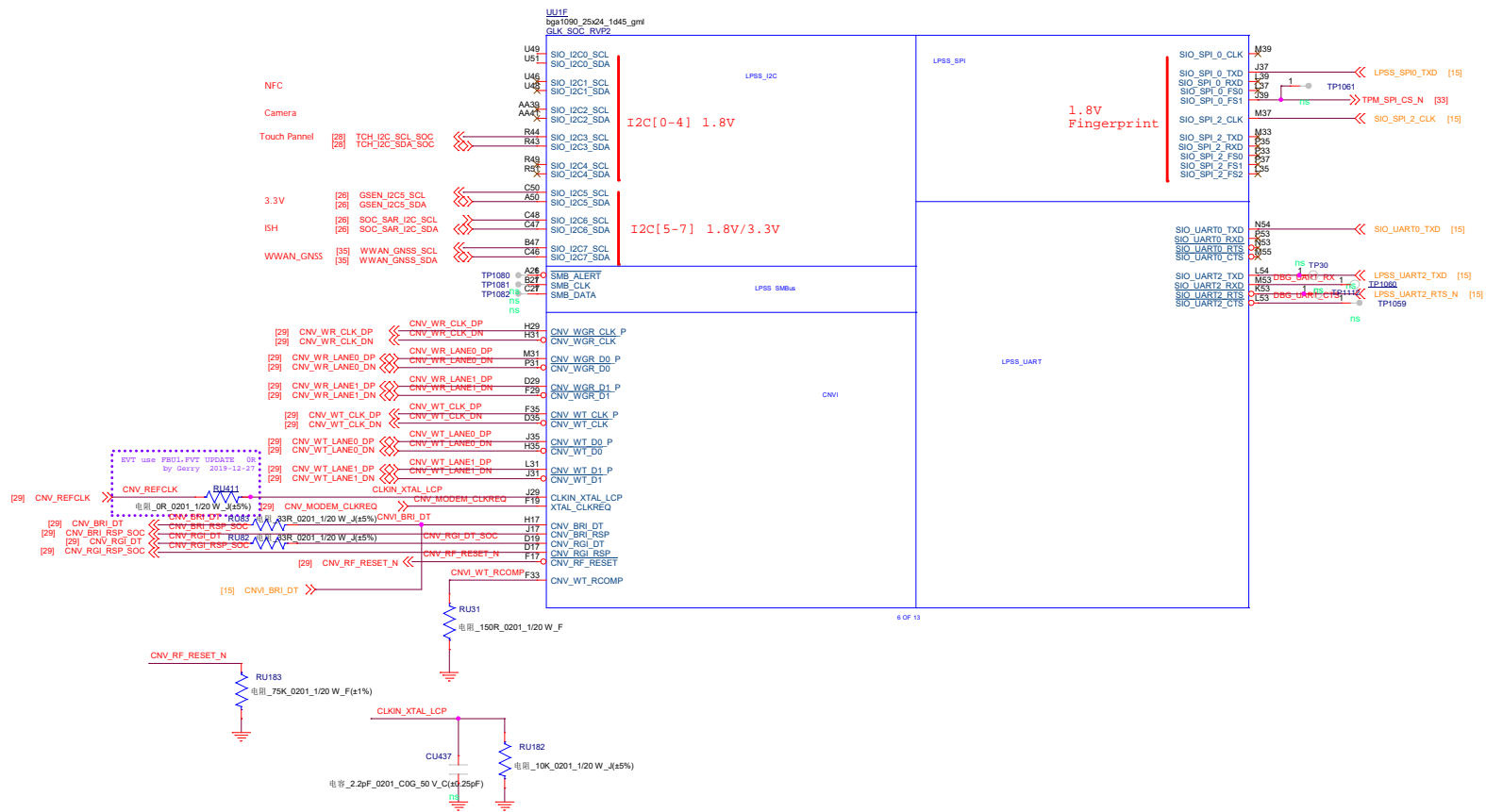
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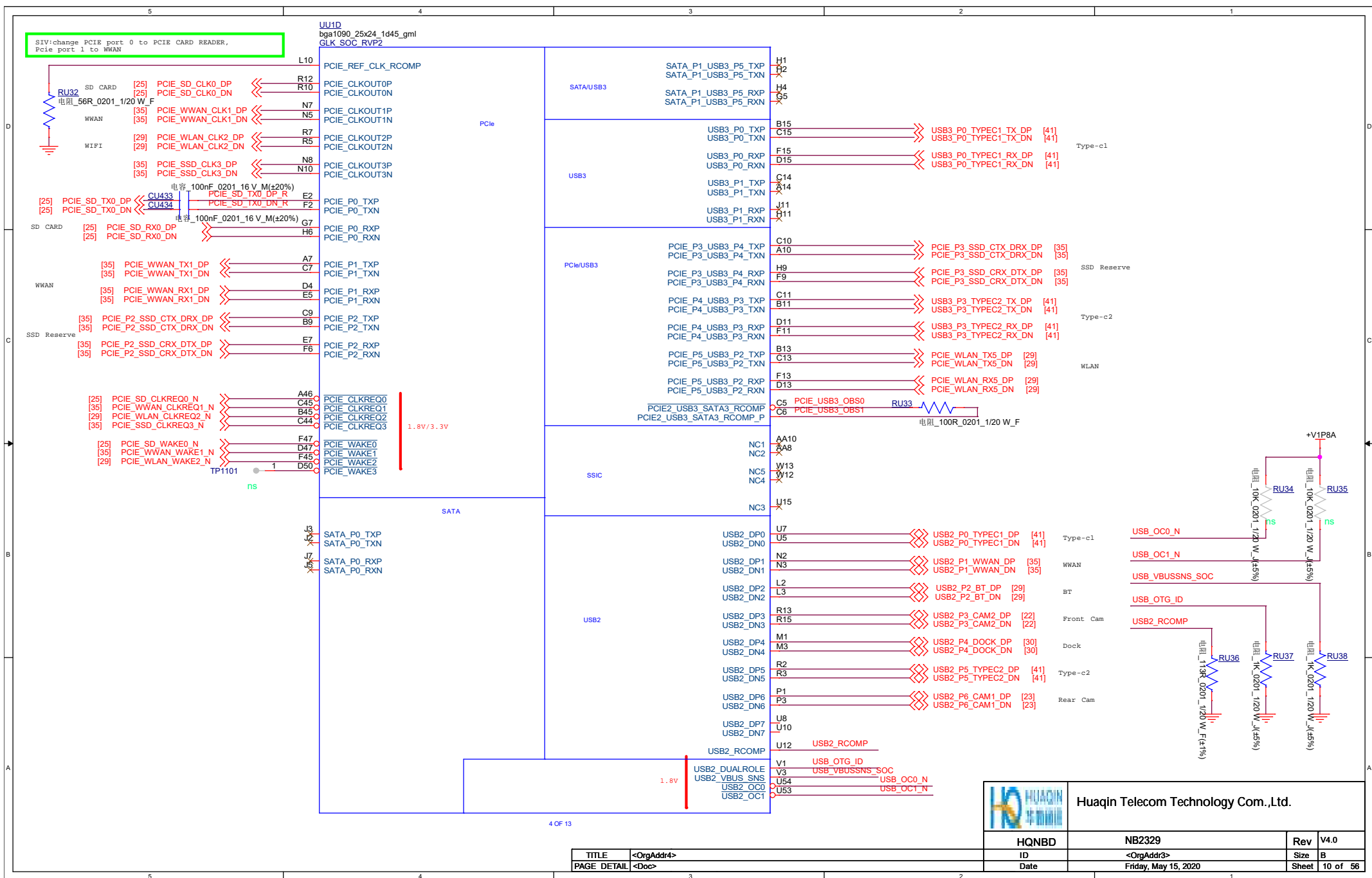
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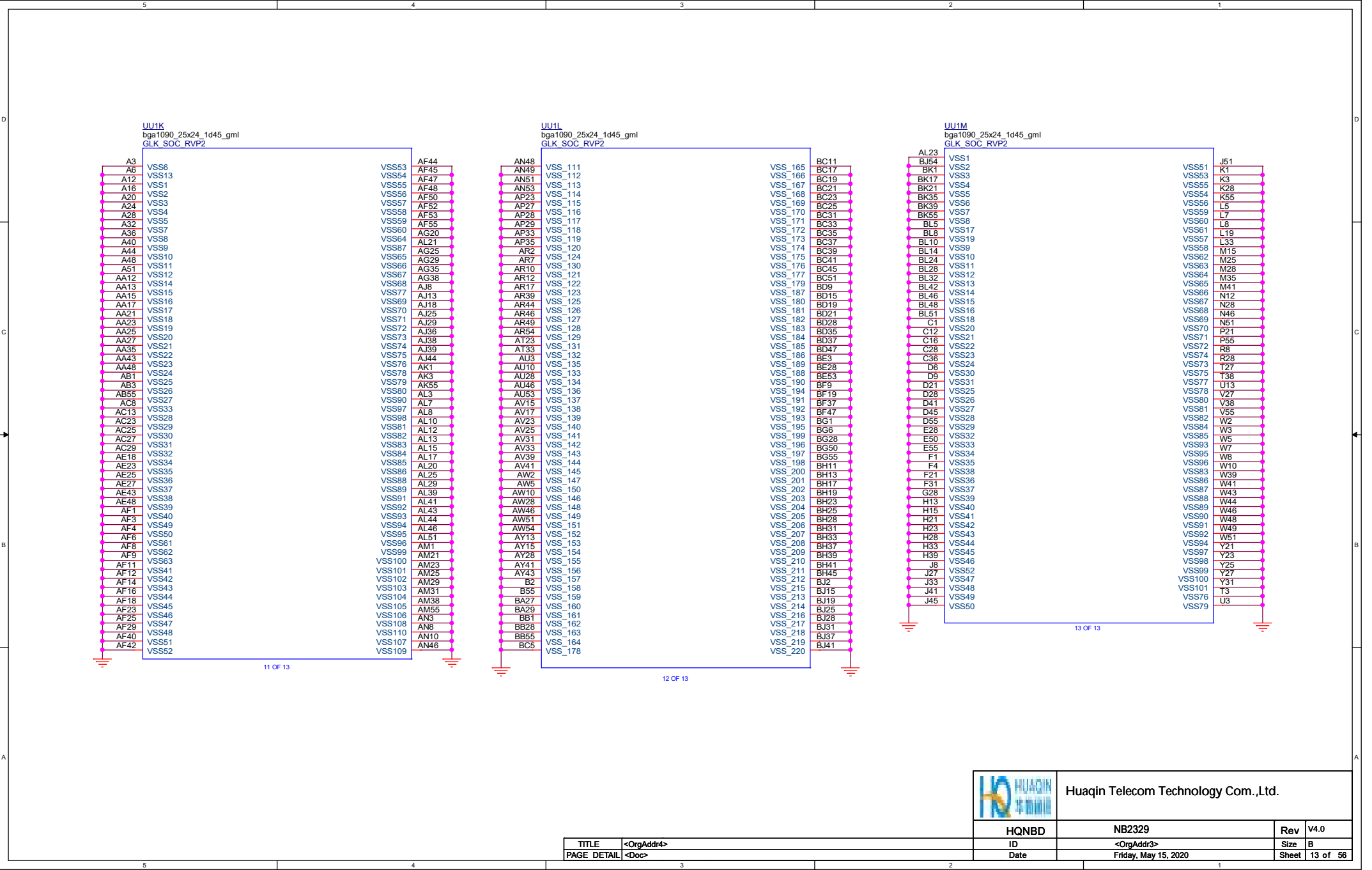


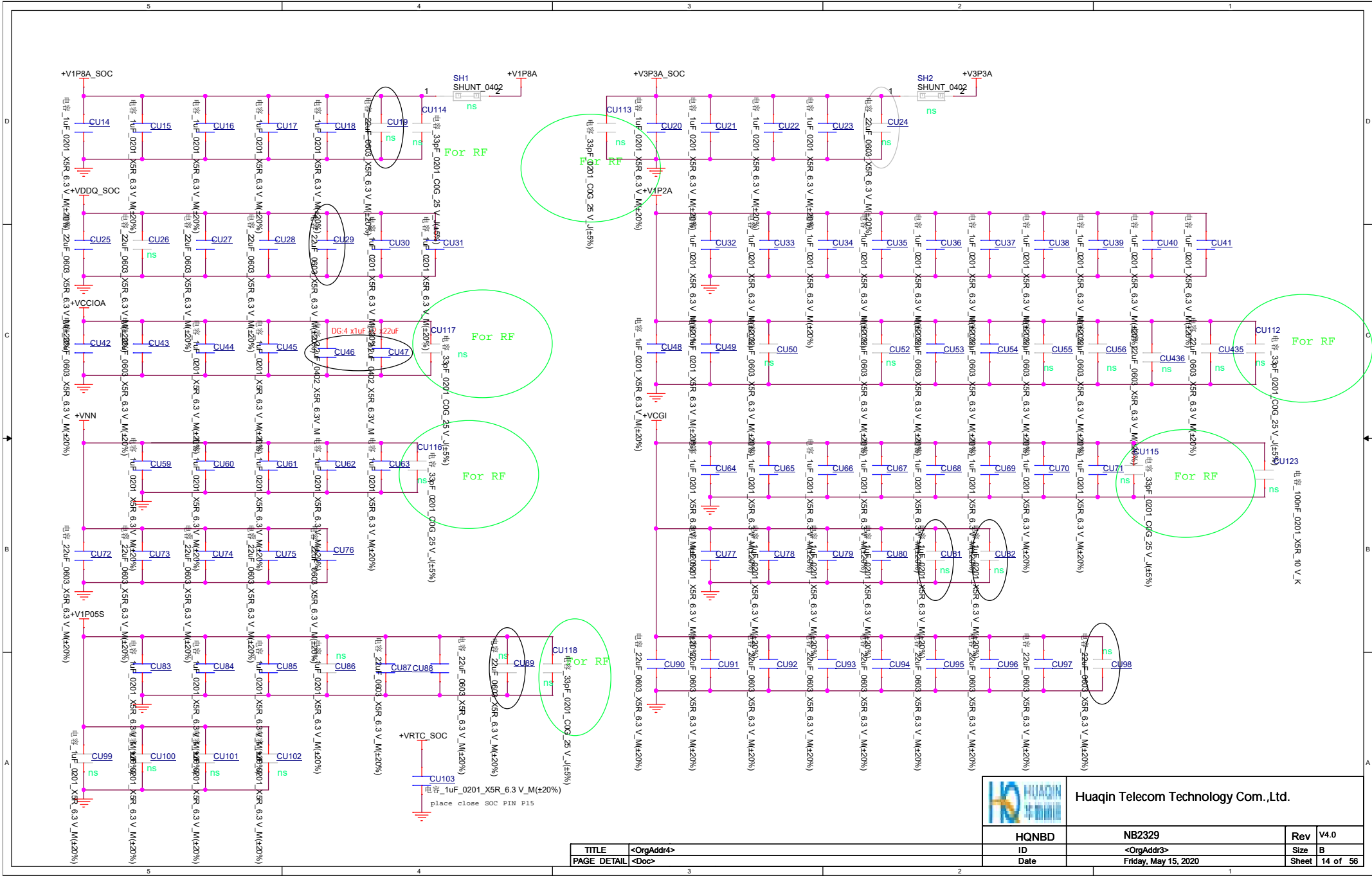










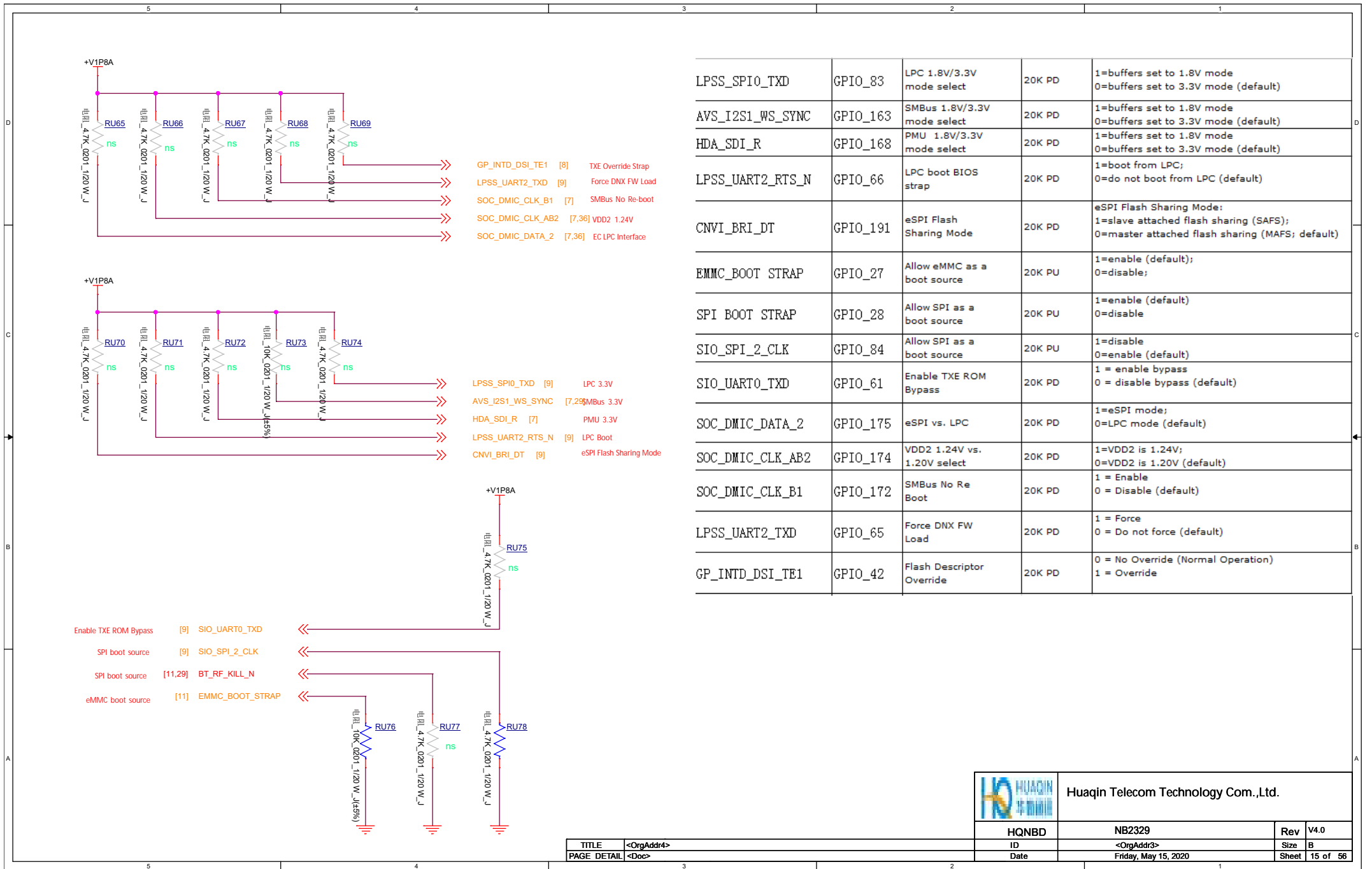


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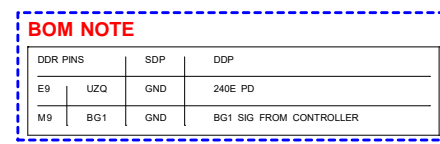
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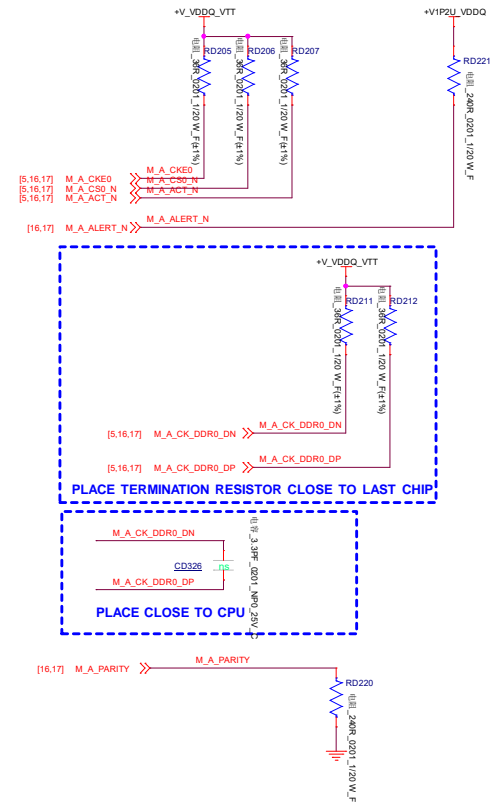
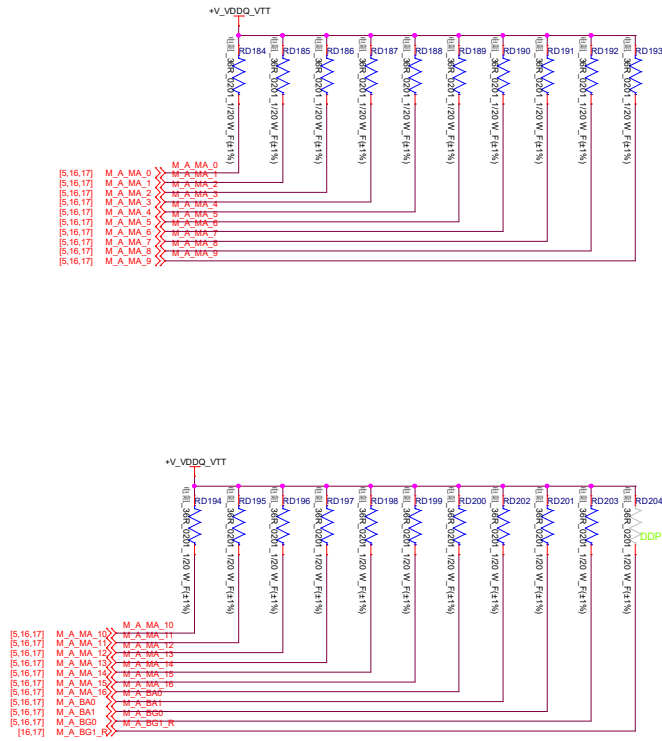






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MEMORY TERMINATIONS MD CHANNEL A

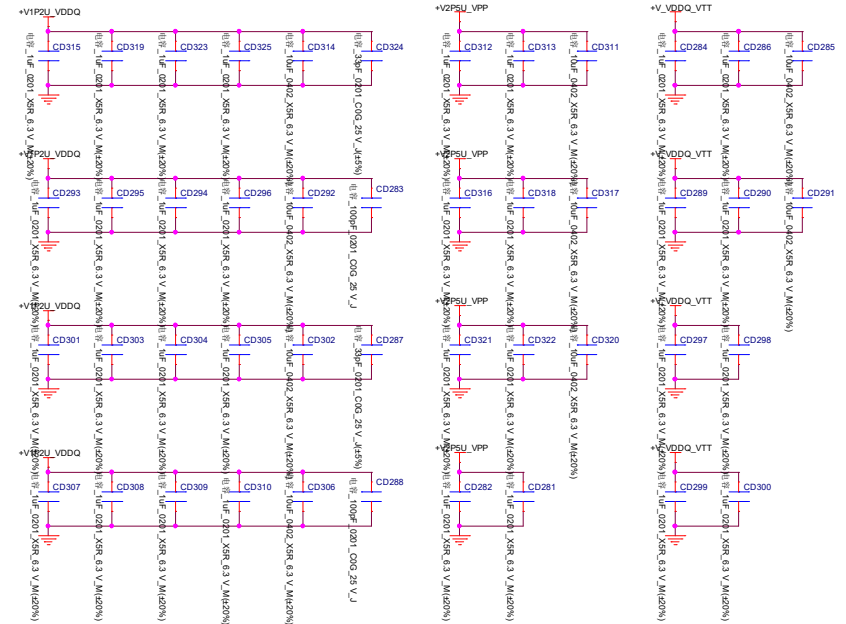


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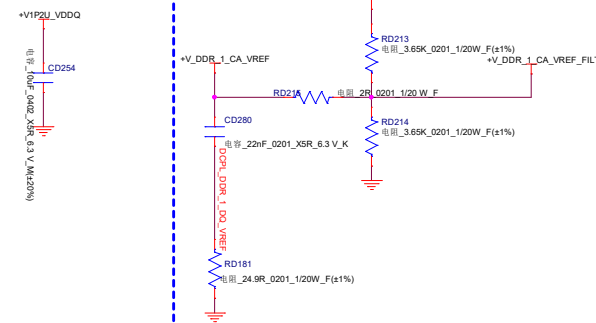
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## DECOUPLING CAPACITORS FOR DDR CHANNEL A



## DDR4 CH A REF GENERATION



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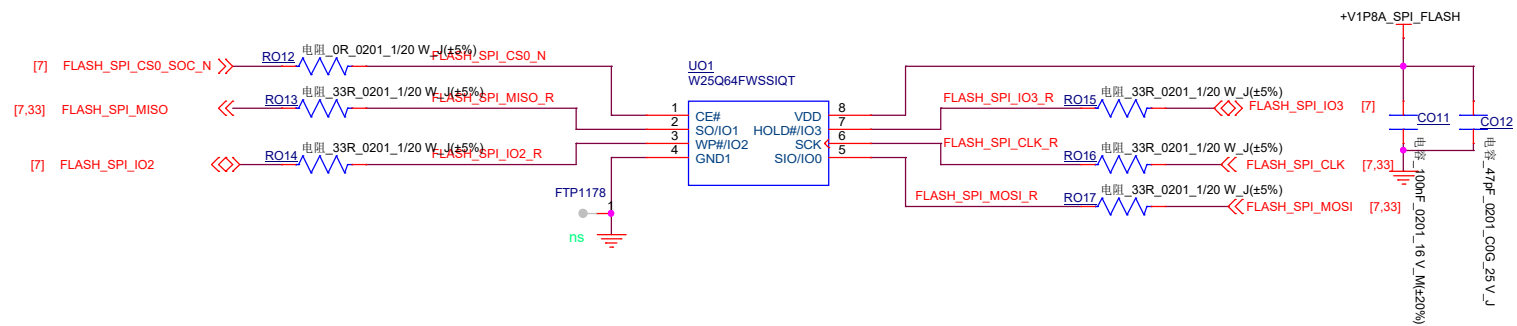
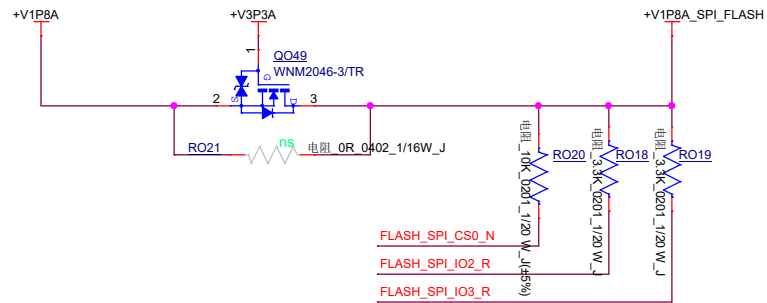
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C

B

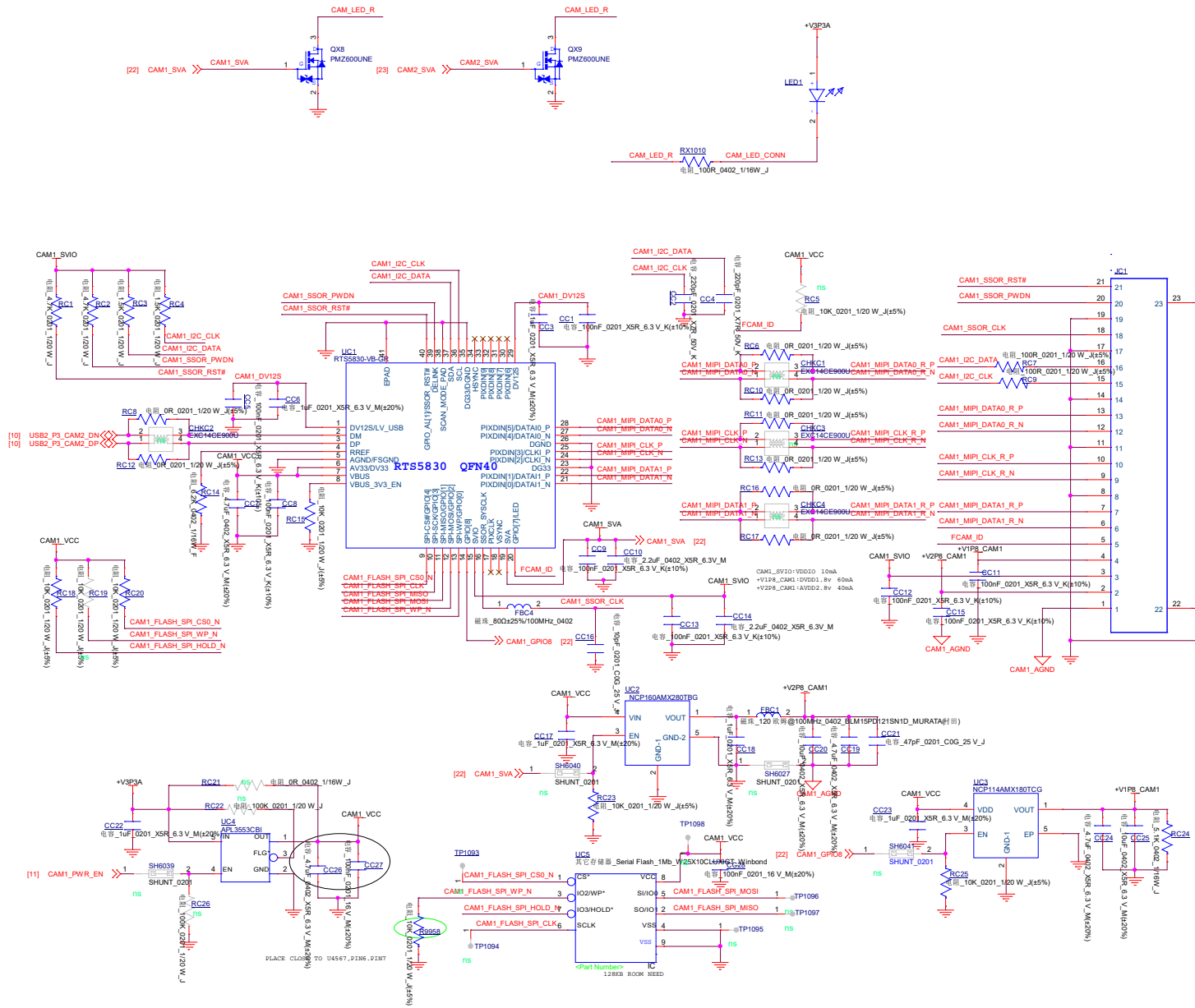
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5 4 3 2 1



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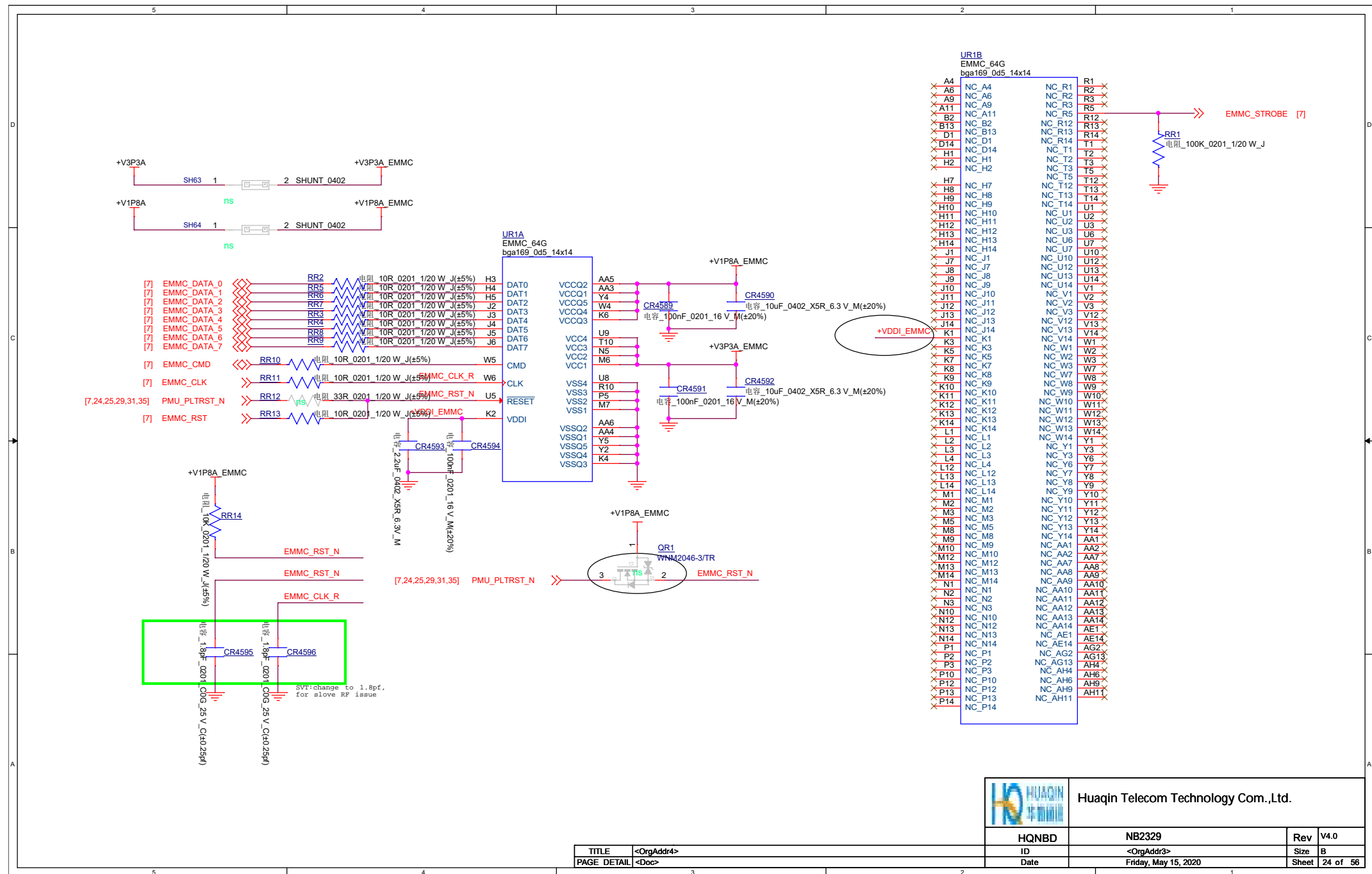


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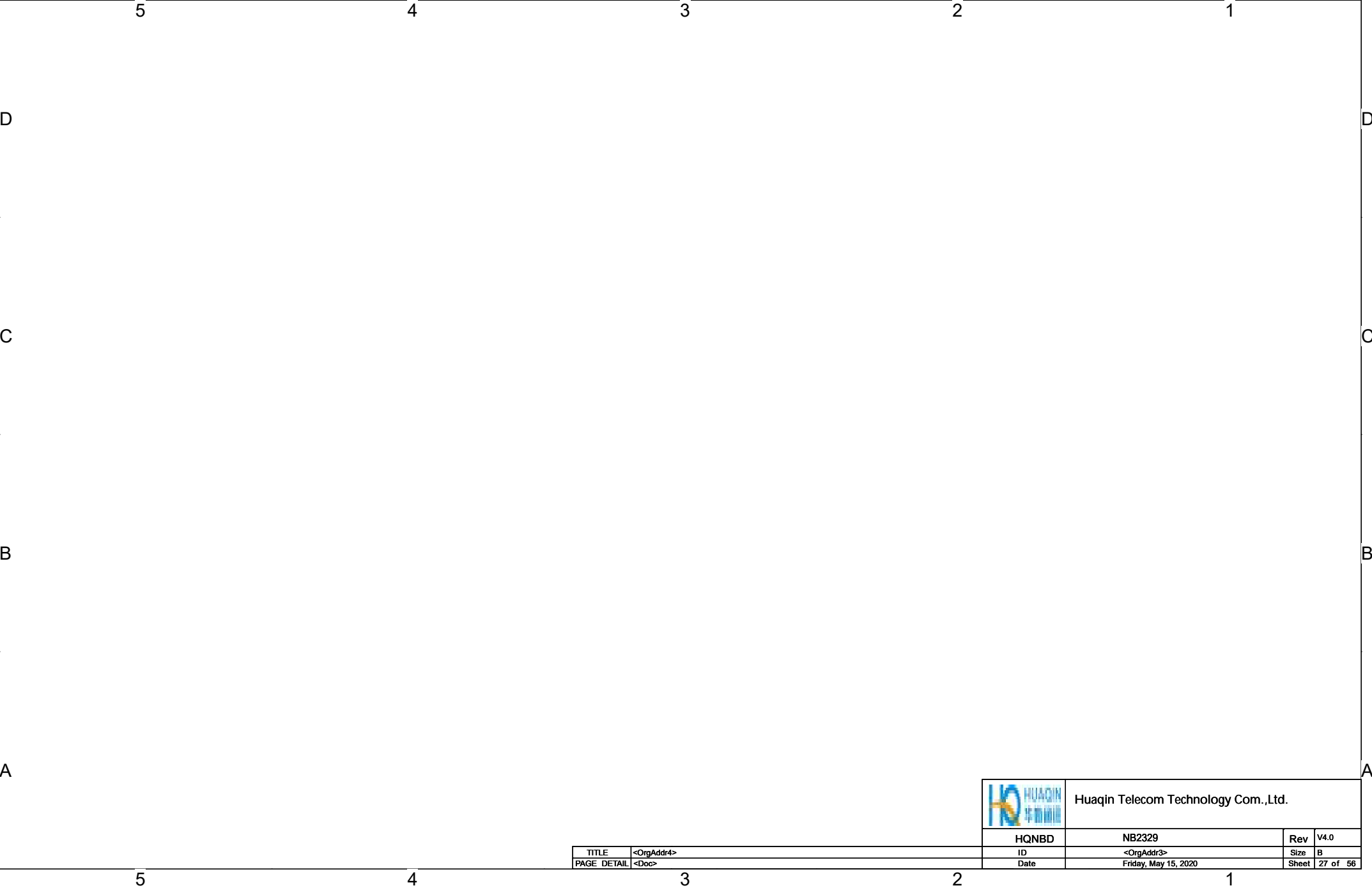
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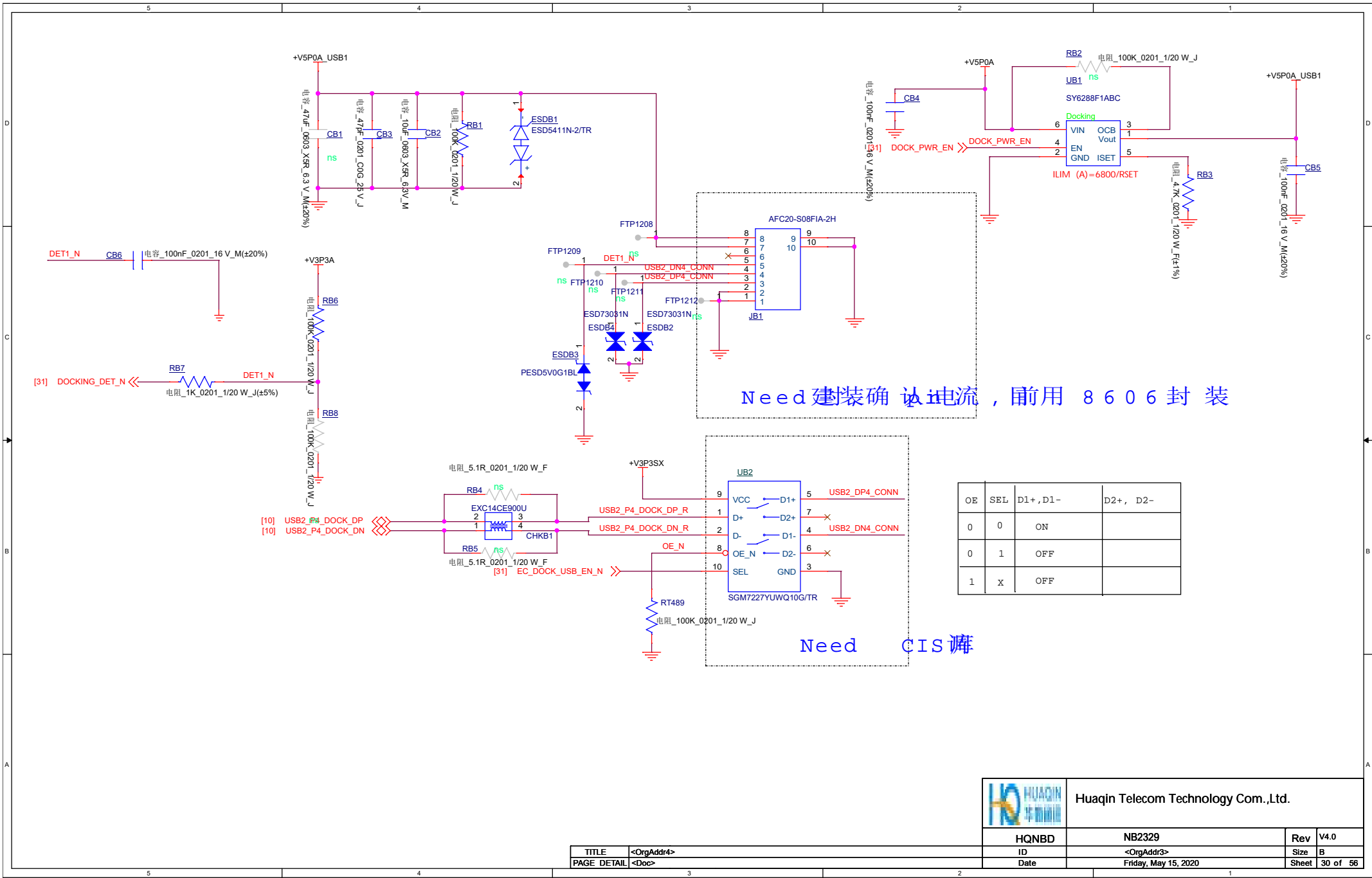


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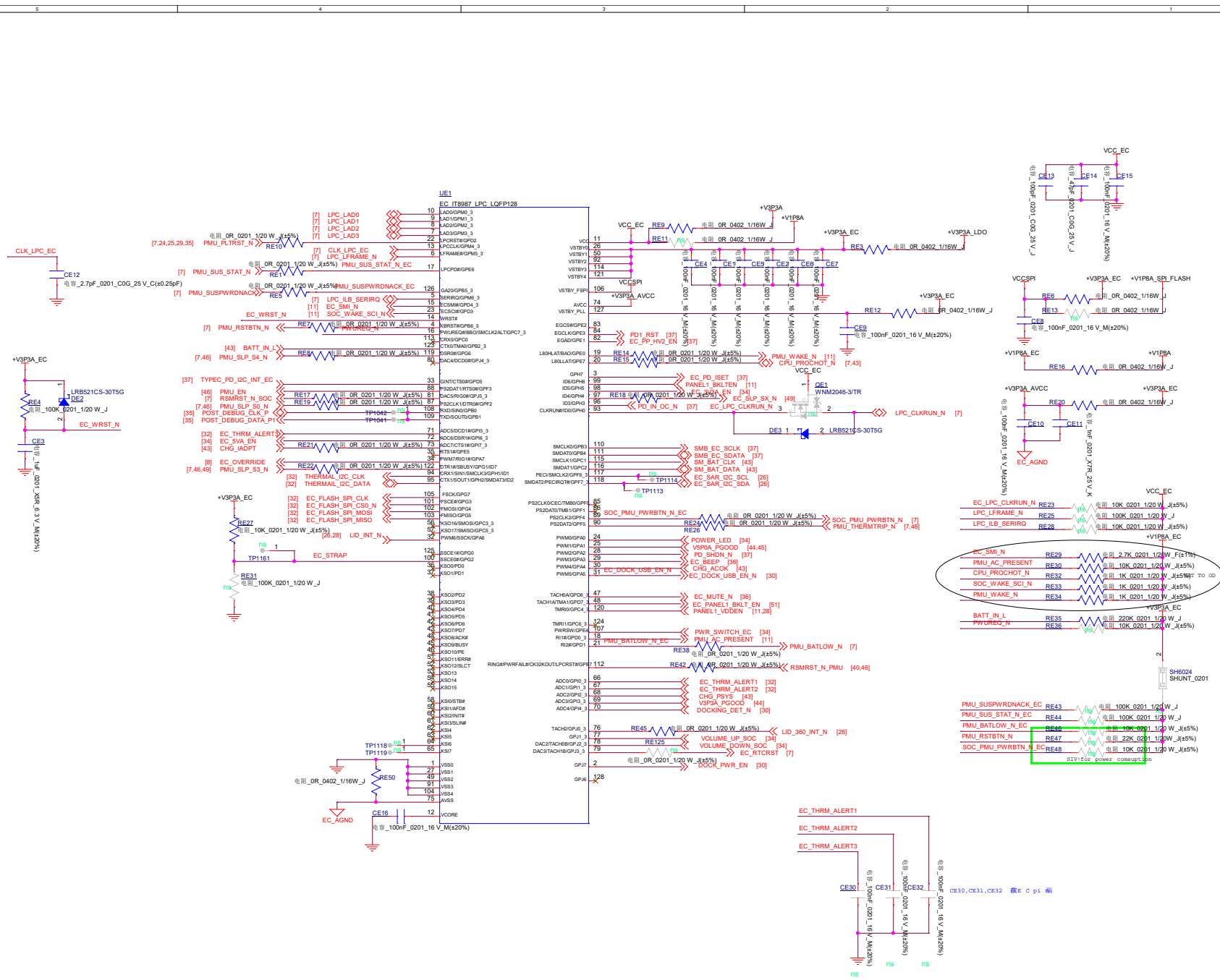


OE	SEL	D1+, D1-	D2+, D2-
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0	1	OFF	
1	X	OFF	

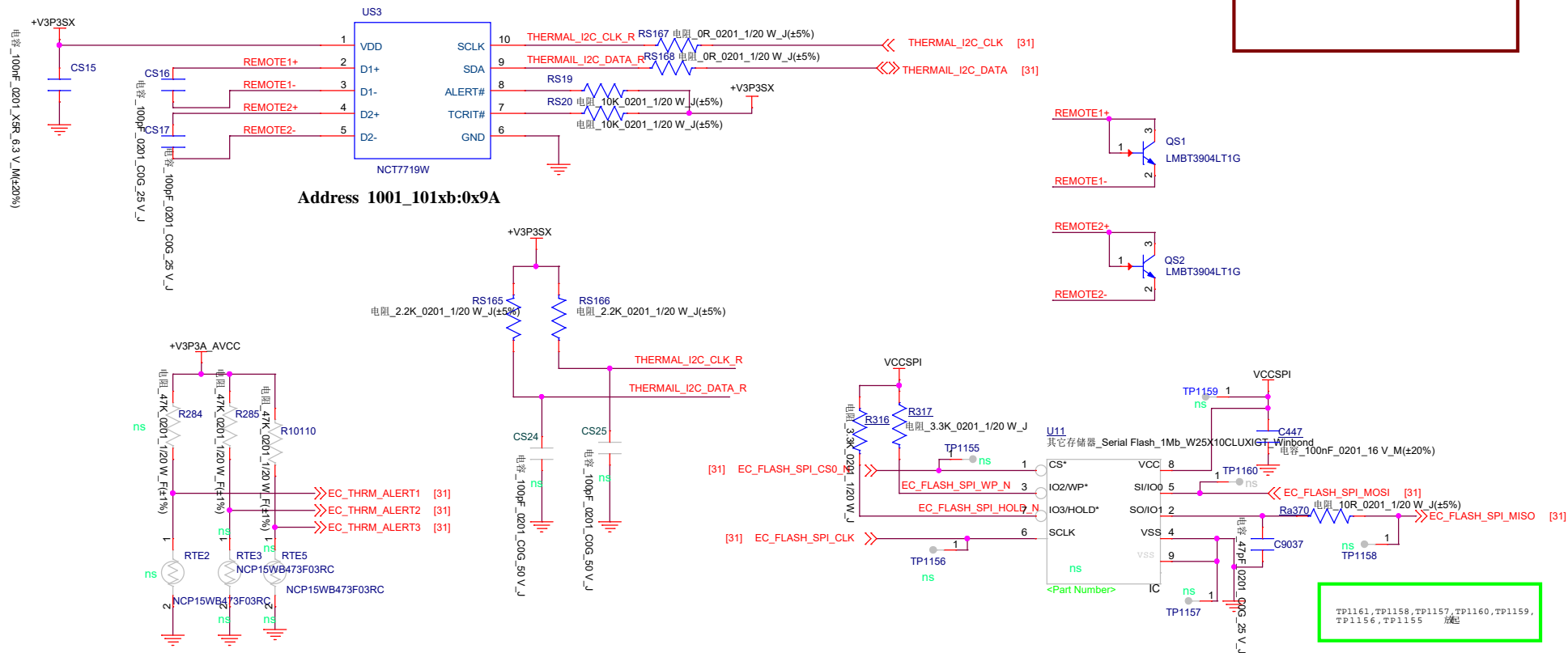



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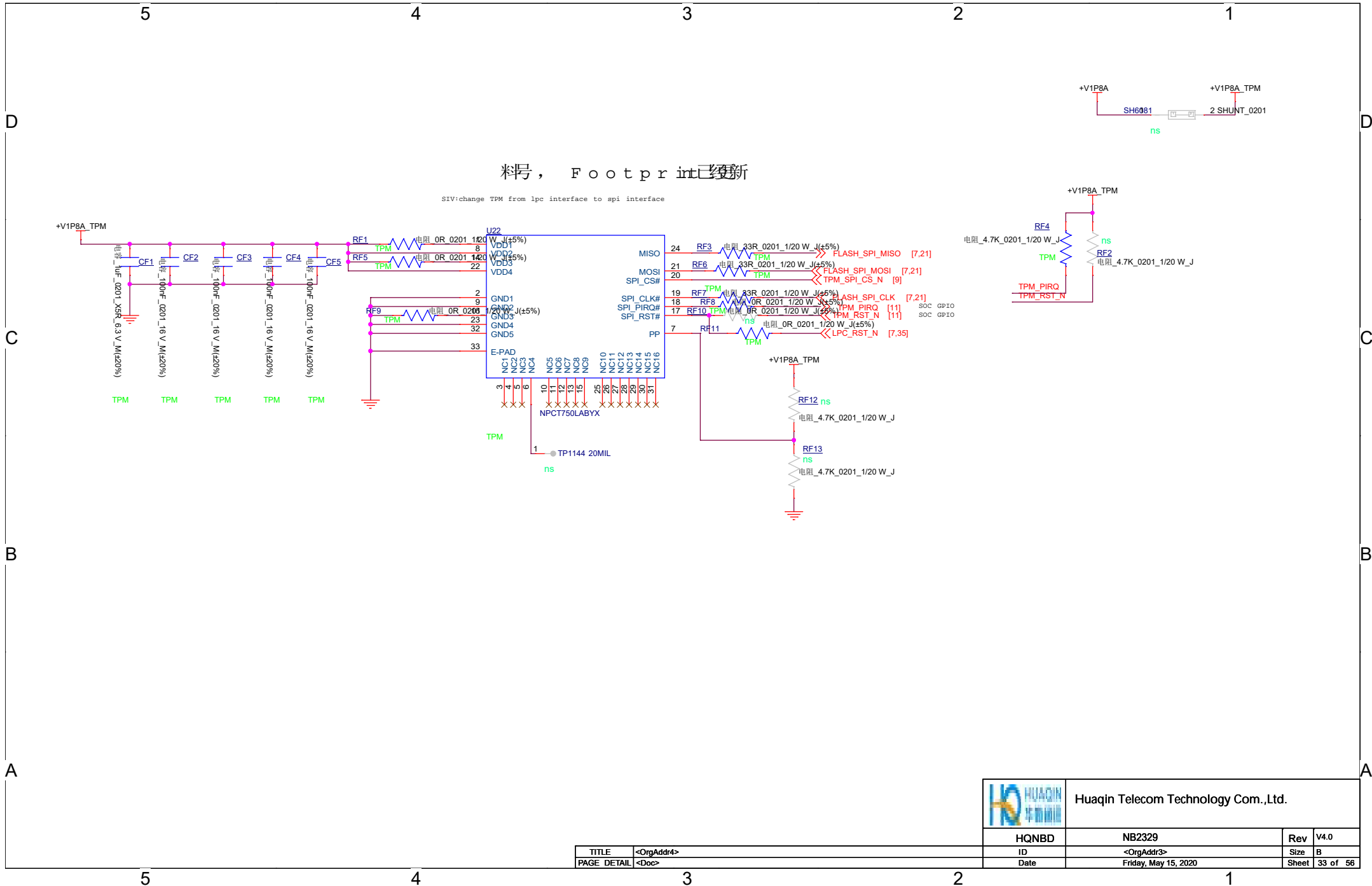
REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"  
Connect guard traces to GND on either side of the  
DXP-DXN traces




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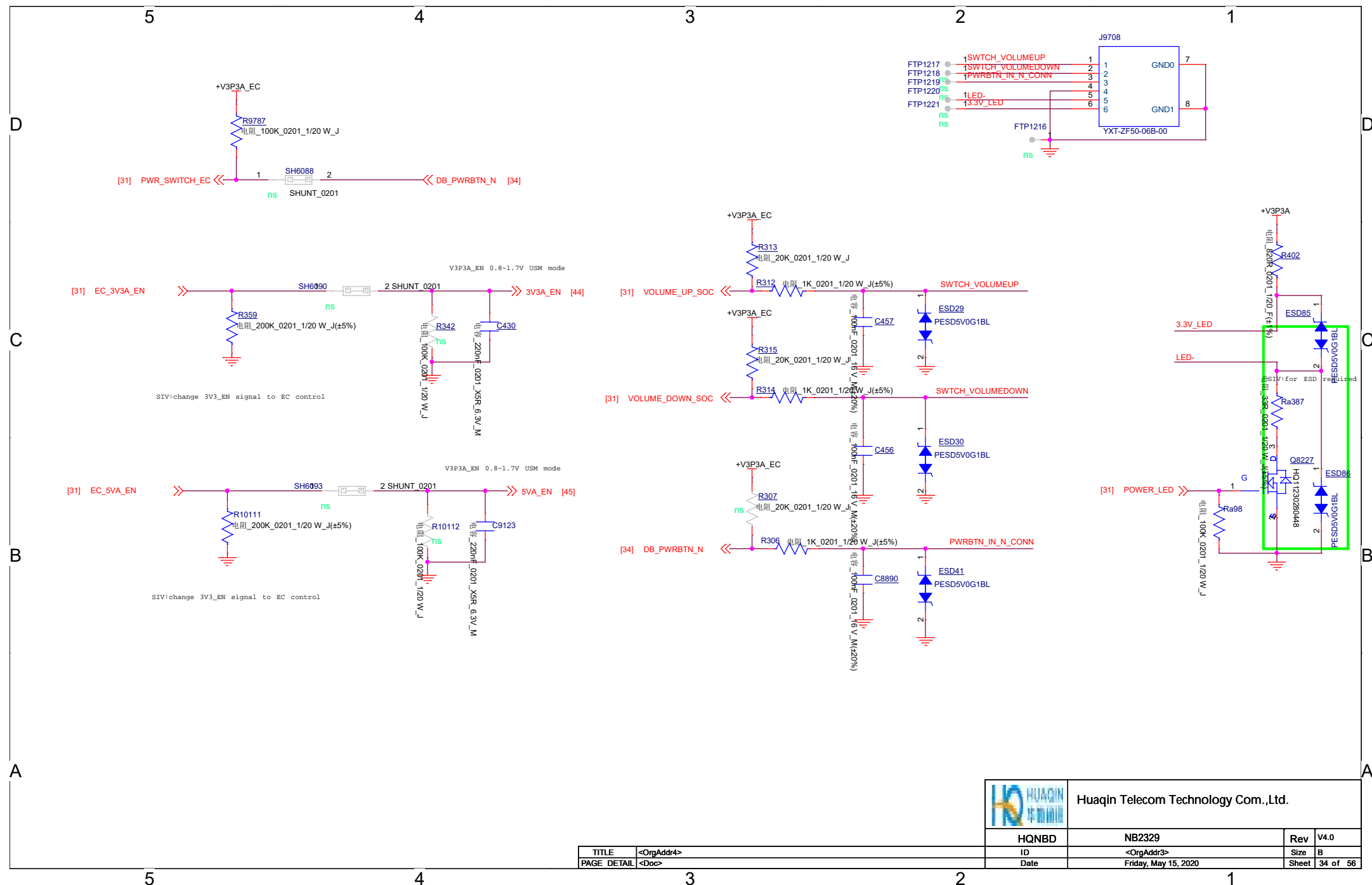
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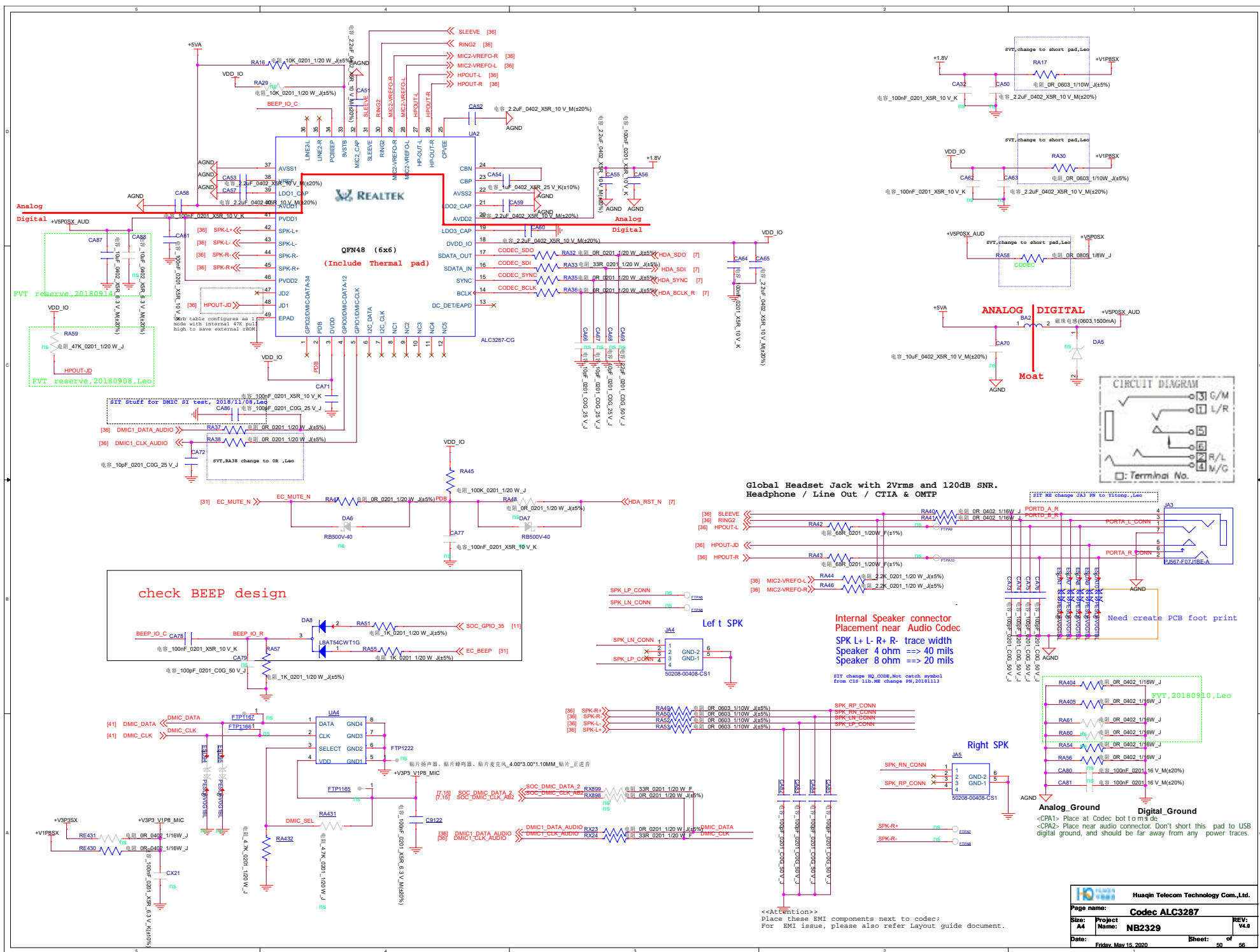
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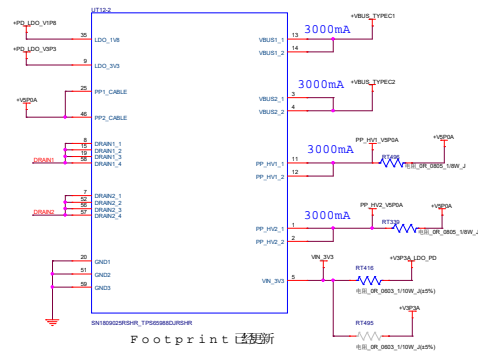
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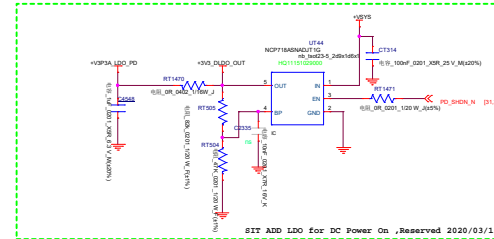
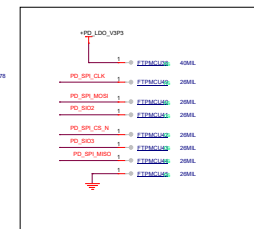
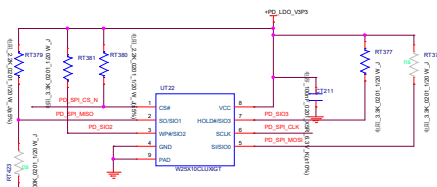
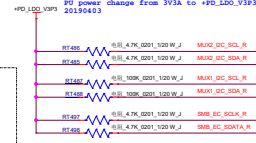
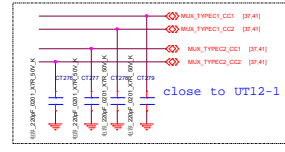
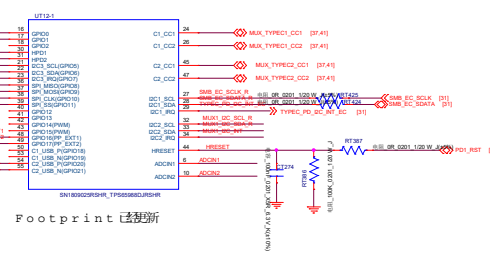
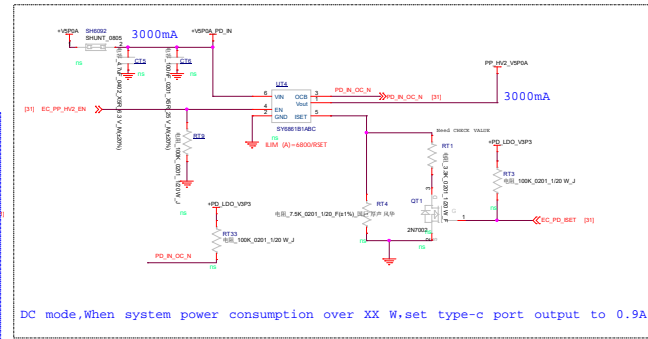
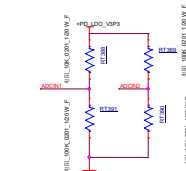
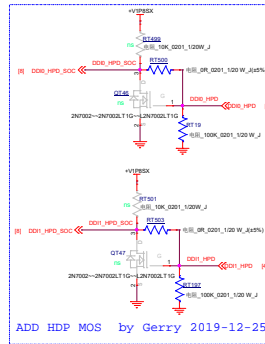
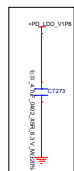
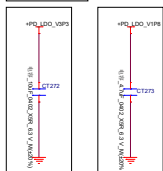
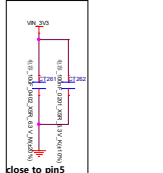
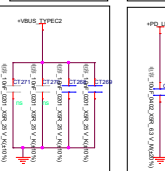
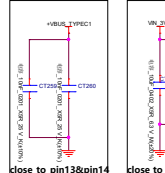
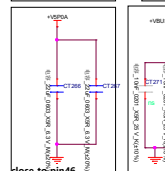
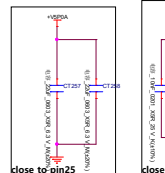
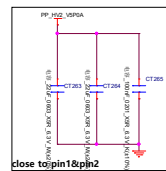
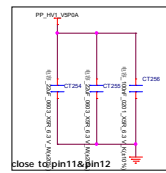




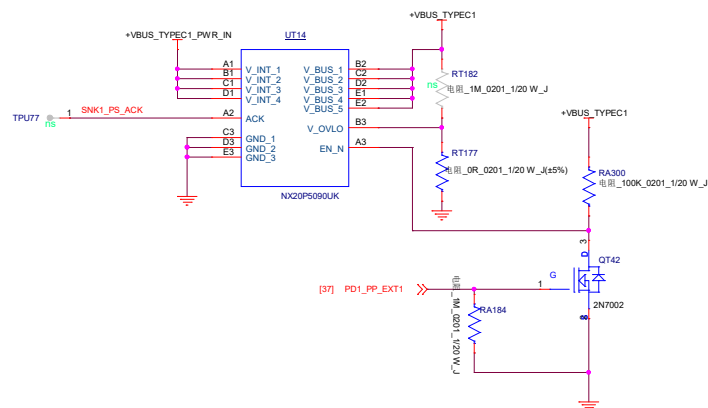
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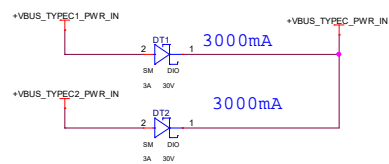
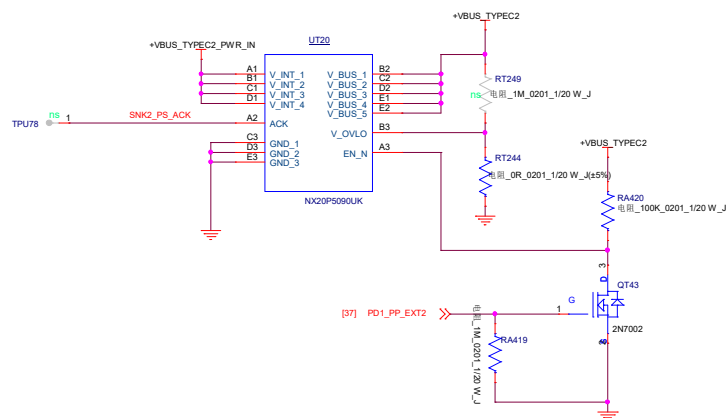
For power off charge




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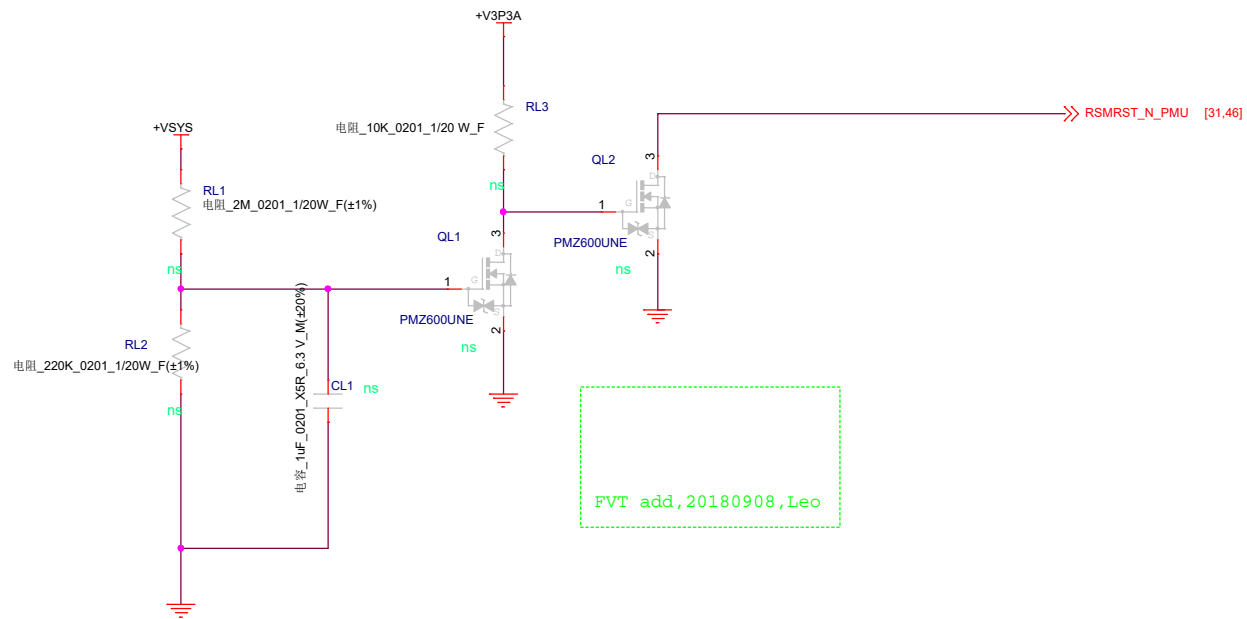


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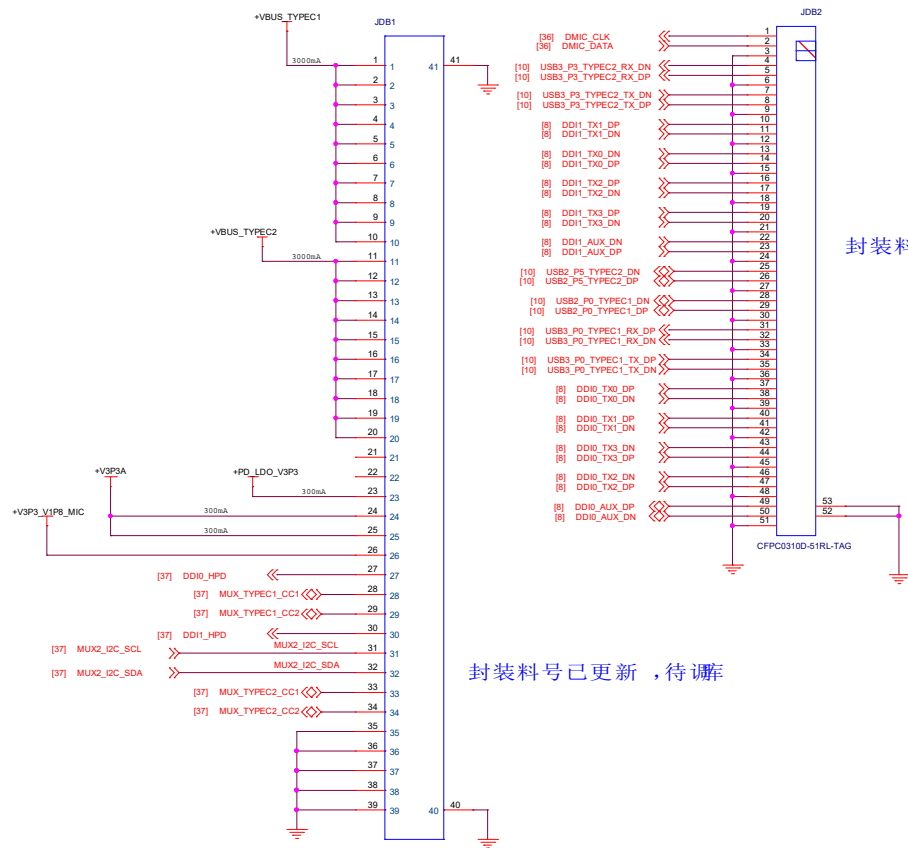


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Type-C 1 CONN

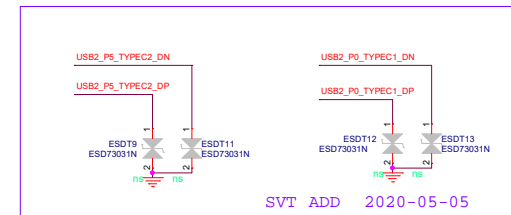






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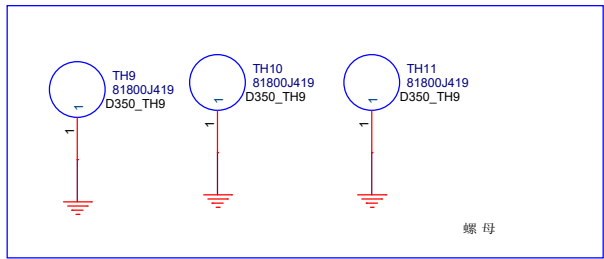
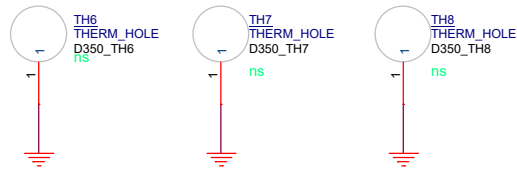
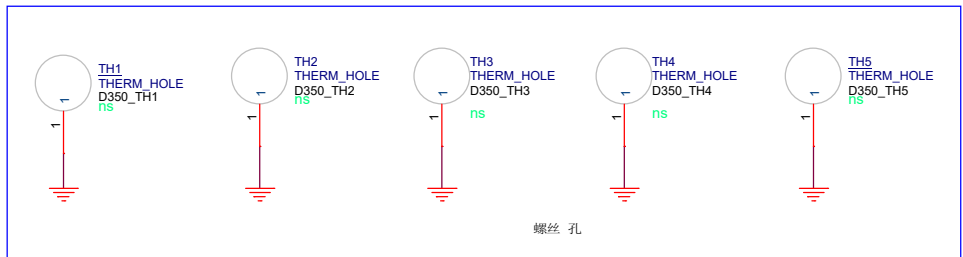
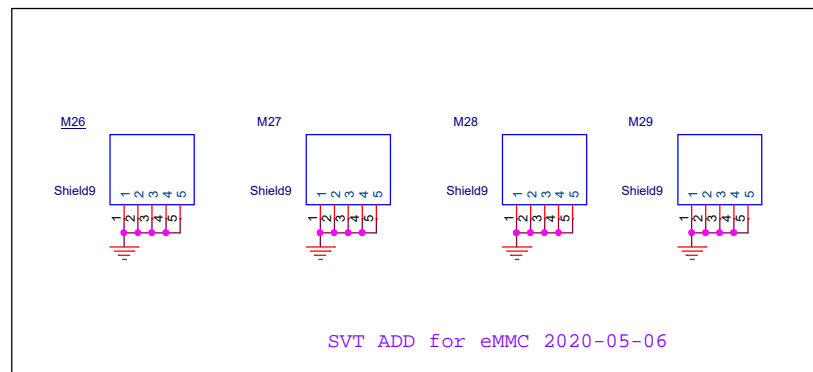
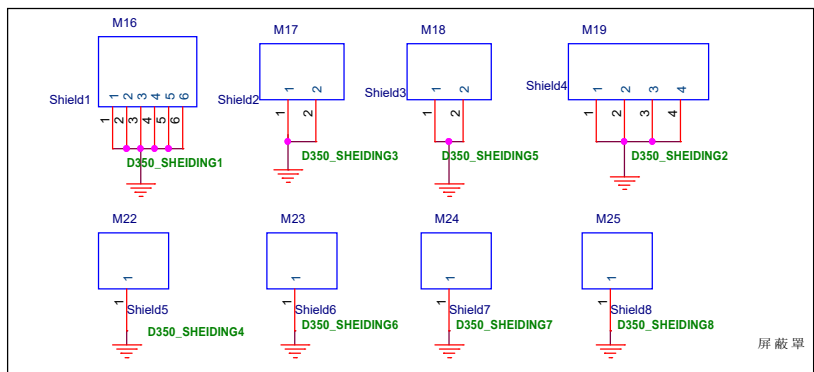
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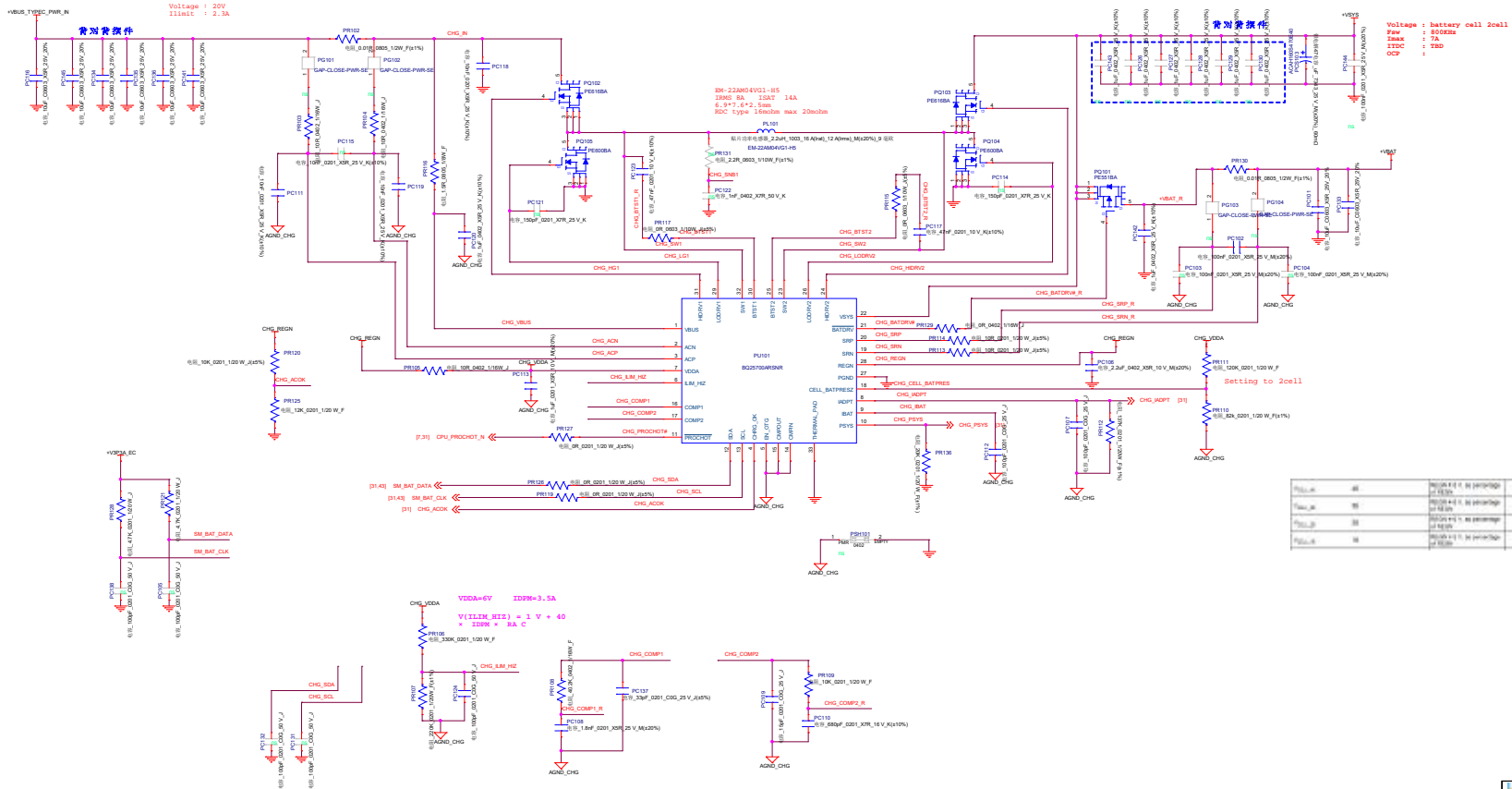
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## Charger



$P_{\text{mean}}$	40	Mean and s.d. percentage of 1000s	44.4%	50%	
$P_{\text{max}}$	95	Mean and s.d. percentage of 1000s	51.1%	95%	95%
$P_{\text{min}}$	30	Mean and s.d. percentage of 1000s	38%	35%	31.7%
$P_{\text{std}}$	10	Mean and s.d. percentage of 1000s	14.6%	10%	11.8%

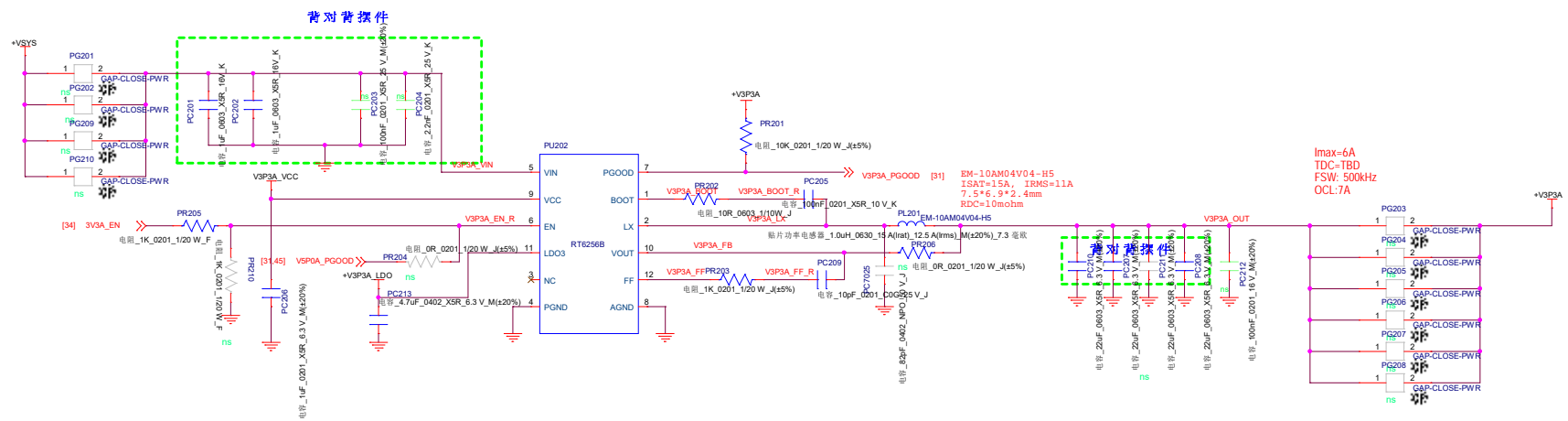
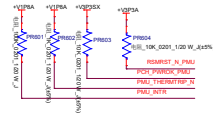


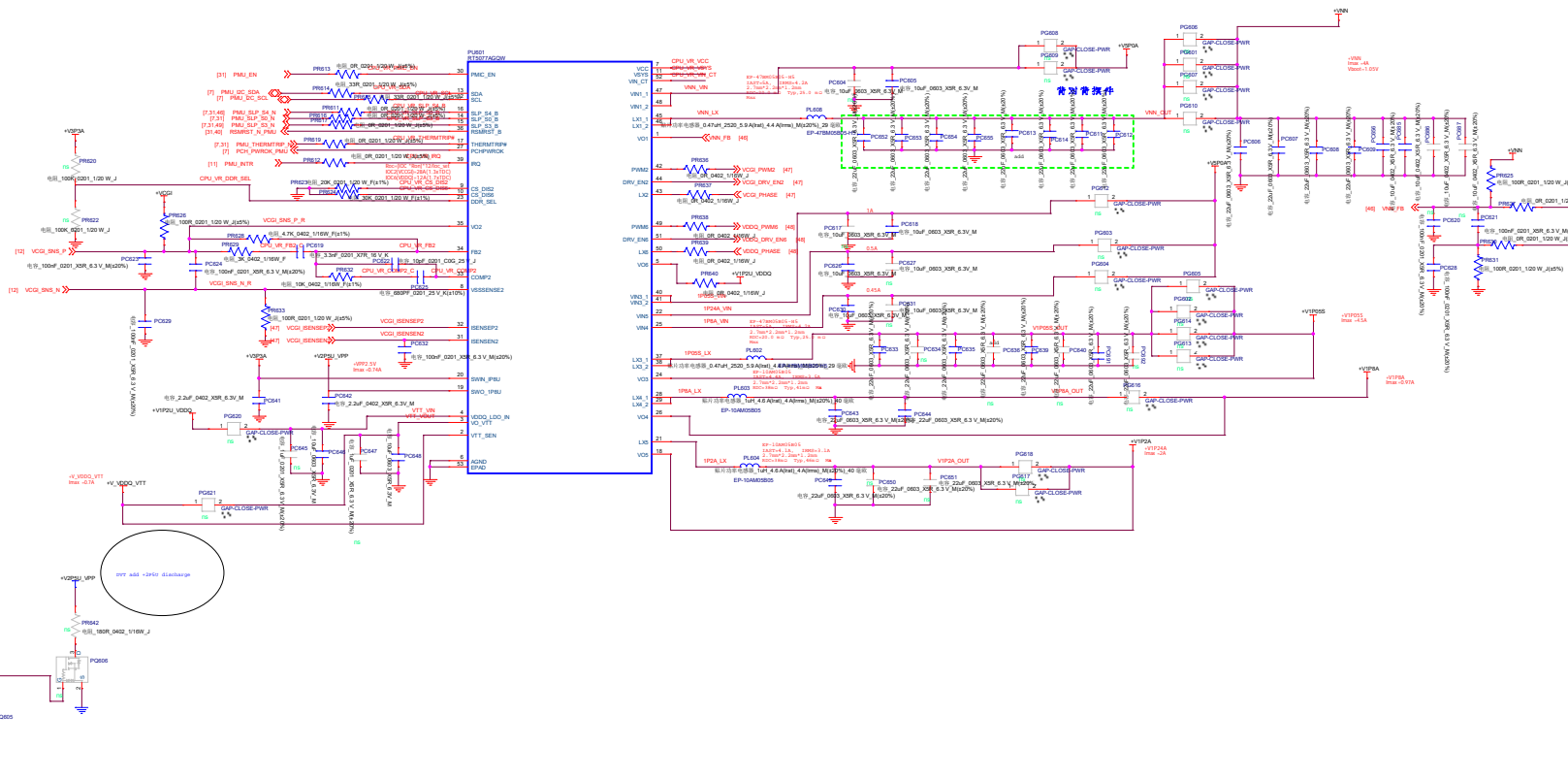
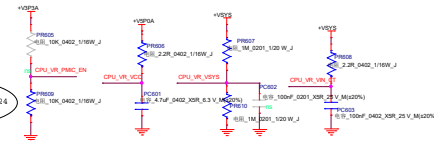


Table 2. Back6 (DDR) Voltage Selection

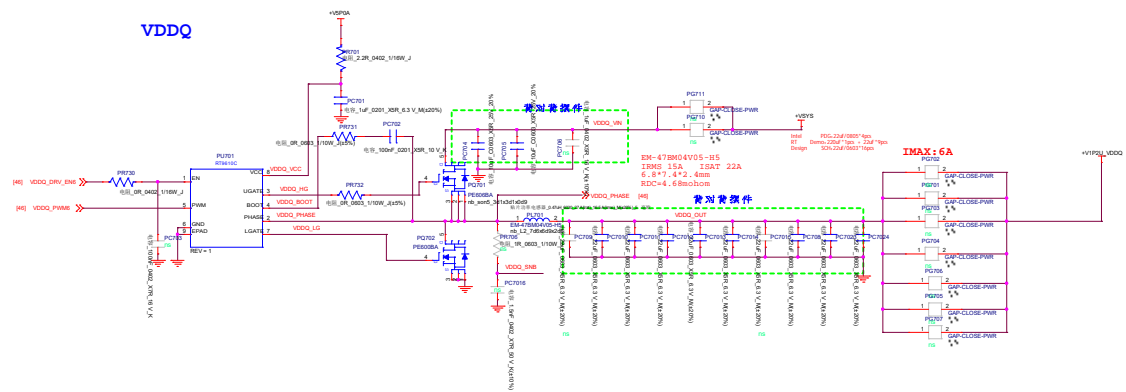
DDR_SEL Pin State	Buck6 Nominal Output Voltage	DDR Technology
H	1.2V	LPDDR3
Floating	1.2V	DDR4 (optional)
L	1.1V	LPDDR4



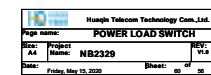
DVT stuff for VBN,20180224

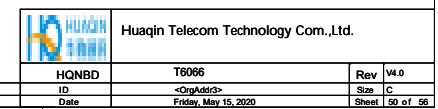











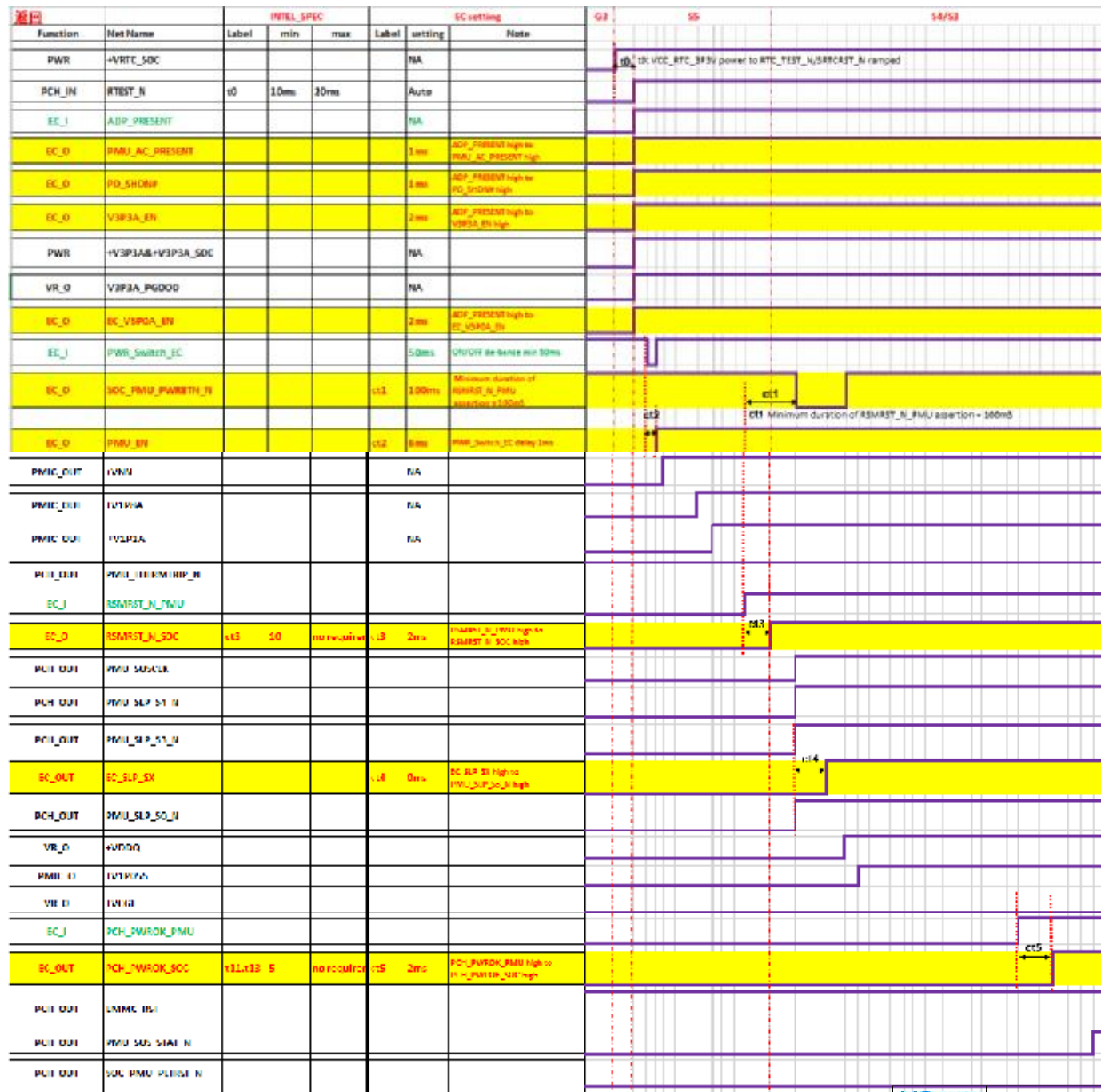




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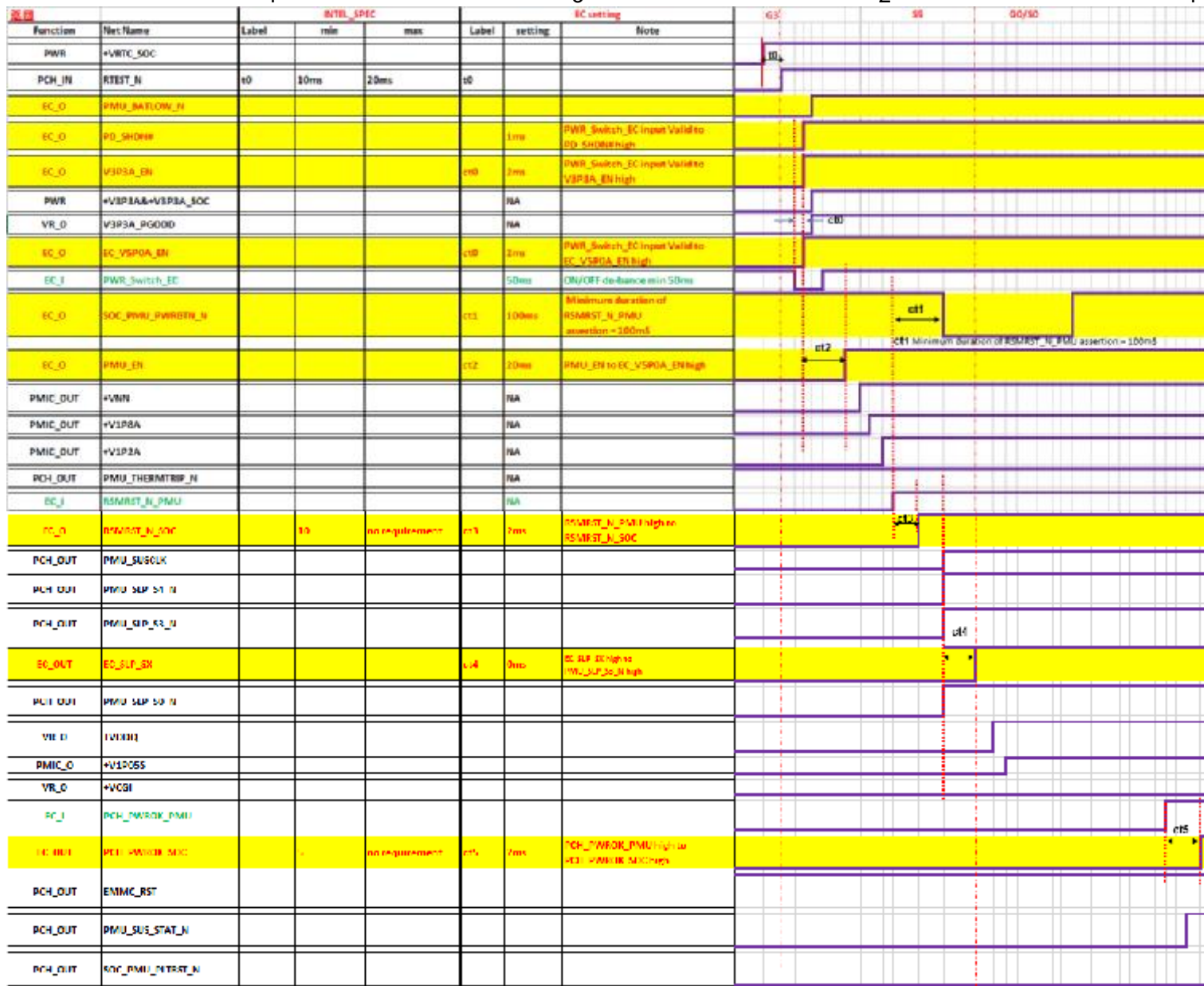
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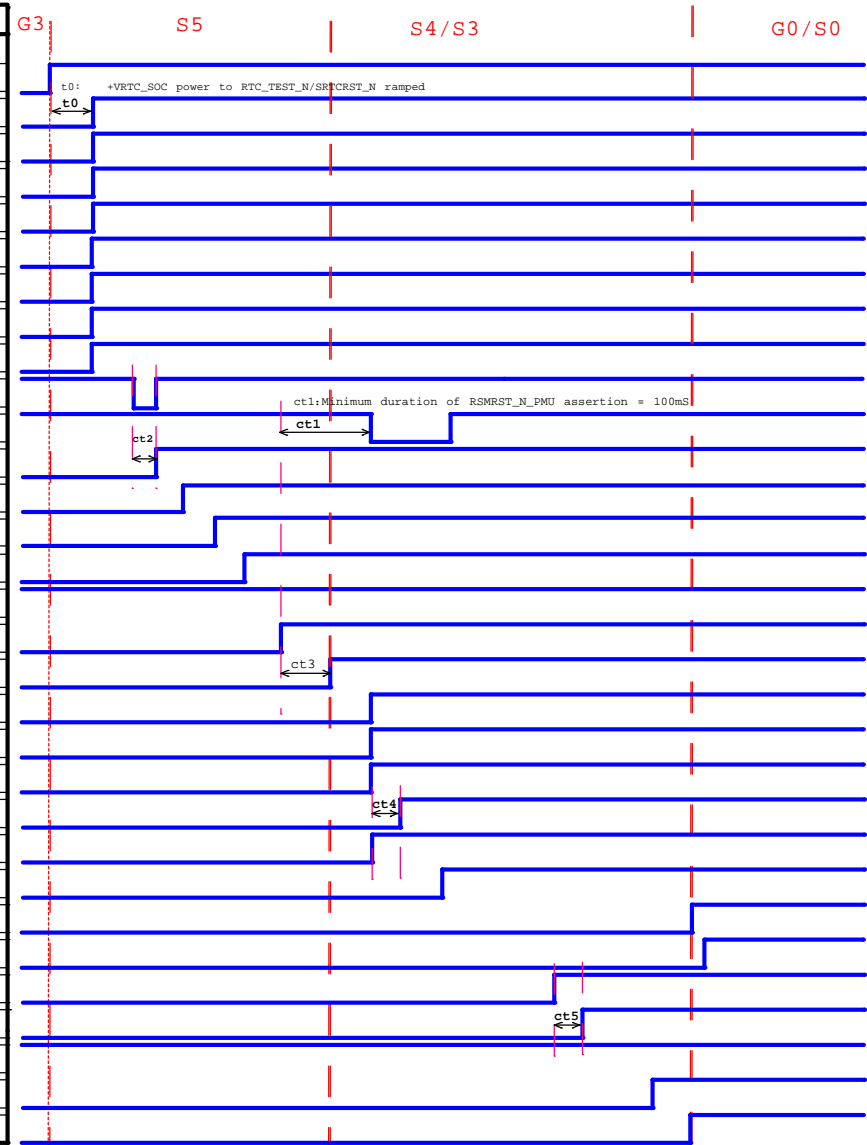
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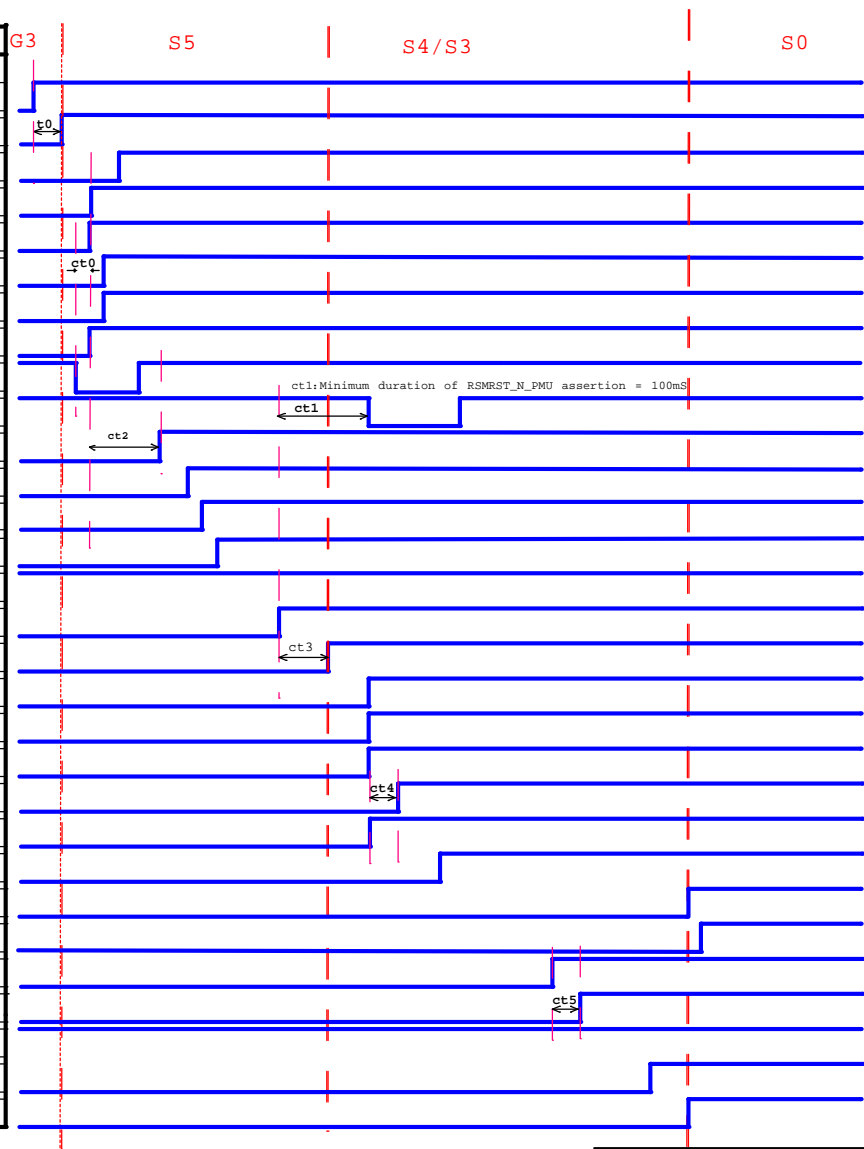
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		Intel_SPEC			EC Setting		
Function	Net Name	Label	Min	Max	Label	Setting	Note
PWR	+VRTC_SOC					NA	
PCH_IN	RTEST_N	t0	10ms	20ms		Auto	
EC_I	ADP_PRESENT					NA	
EC_O	PMU_AC_PRESENT					1ms	ADP_PRESENT High to PMC_AC_PRESENT High
EC_O	PD_SHDN#					1ms	PMC_AC_PRESENT High to PD_SHDN# High
EC_O	+V3P3A_EN					2ms	PD_SHDN# High to +V3P3A_EN
PWR	+V3P3A&+V3P3A_SOC					NA	
VR_O	+V3P3A_PGOOD					NA	
EC_O	EC_+V5P0A_EN					2ms	ADP_PRESENT High to EC_+V5P0A_EN High
EC_I	PWR_Switch_EC					50ms	ON/OFF de-bounce min 50ms
EC_O	SOC_PMU_PWRBTN_N				ct1	100ms	Minimum duration of RSMRST_N_PMU assertion = 100ms
EC_O	PMU_EN				ct2	6ms	PWR_Switch_EC delay 1ms
PMIC_OUT	+VNN					NA	
PMIC_OUT	+V1P8A					NA	
PMIC_OUT	+V1P2A						
PMIC_OUT	PMU_THERMTRIP_N					NA	
EC_I	RSMRST_N_PMU						
EC_O	RSMRST_N_SOC	ct3	10ms	NA	ct3	10ms	RSMRST_N_PMU High to RSMRST_N_SOC High
PCH_OUT	PMU_SUSCLK						
PCH_OUT	PMU_SLP_S4_N						
PCH_OUT	PMU_SLP_S3_N						
EC_OUT	EC_SLP_SX				ct4	0ms	PMU_SLP_S3_N high to EC_SLP_SX high
PCH_OUT	PMU_SLP_S0_N						
VR_O	+VDDQ						
PMIC_O	+V1P05S						
VR_O	+VCCGI						
EC_I	PCH_PWROK_PMU						
EC_O	PCH_PWROK_SOC	t11,t13	5ms	NA	ct5	2ms	PCH_PWROK_PMU high to PCH_PWROK_SOC high
PCH_OUT	PCH_PWROK_SOC						
PCH_OUT	PMU_SUS_STAT_N						
PCH_OUT	SOC_PMU_PLTRST_N						



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		Intel_SPEC			EC Setting		
Function	Net Name	Label	Min	Max	Label	Setting	Note
PWR	+VRTC_SOC						
PCH_IN	RTEST_N	t0	10ms	20ms			
EC_O	PMU_BATLOW_N						
EC_O	PD_SHDN#					1ms	PWR_Switch_EC input Valid to PD_SHDN# High
EC_O	+V3P3A_EN				ct0	2ms	PWR_Switch_EC input Valid to +V3P3A_EN
PWR	+V3P3A&+V3P3A_SOC					NA	
VR_O	+V3P3A_PGOOD					NA	
EC_O	EC_+V5P0A_EN				ct0	2ms	PWR_Switch_EC input Valid to EC_+V5P0A_EN High
EC_I	PWR_Switch_EC					50ms	ON/OFF de-bance min 50ms
EC_O	SOC_PMU_PWRBTN_N				ct1	100ms	Minimum duration of RSMRST_N_PMU assertion = 100ms
EC_O	PMU_EN				ct2	20ms	PMU_EN to +V5P0A_EN High
PMIC_OUT	+VNN					NA	
PMIC_OUT	+V1P8A					NA	
PMIC_OUT	+V1P2A						
PMIC_OUT	PMU_THERMTRIP_N					NA	
EC_I	RSMRST_N_PMU						
EC_O	RSMRST_N_SOC	ct3	10ms	NA	ct3	10ms	RSMRST_N_PMU High to RSMRST_N_SOC High
PCH_OUT	PMU_SUSCLK						
PCH_OUT	PMU_SLP_S4_N						
PCH_OUT	PMU_SLP_S3_N						
EC_OUT	EC_SLP_SX				ct4	0ms	PMU_SLP_S3_N high to EC_SLP_SX high
PCH_OUT	PMU_SLP_S0_N						
VR_O	+VDDQ						
PMIC_O	+V1P05S						
VR_O	+VCCG1						
EC_I	PCH_PWROK_PMU						
EC_O	PCH_PWROK_SOC	t11,t13	5ms	NA	ct5	2ms	PCH_PWROK_PMU high to PCH_PWROK_SOC high
PCH_OUT	PCH_PWROK_SOC						
PCH_OUT	PMU_SUS_STAT_N						
PCH_OUT	SOC_PMU_PLTRST_N						



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